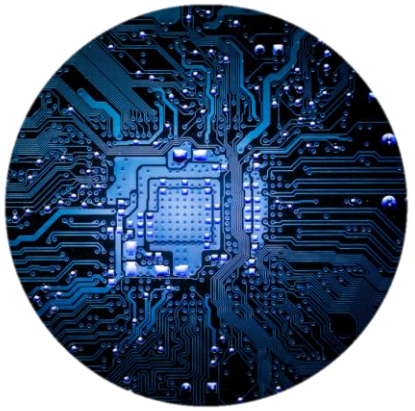
UNIVERSIDAD DE BURGOS

Lesson 2: Logic families

José M. Cámara and Miguel Cantera

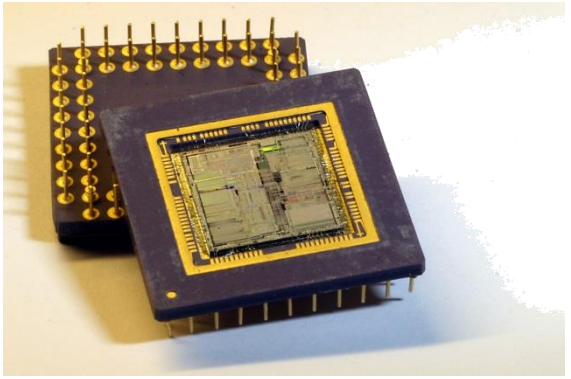
(checam@ubu.es and macantera@ubu.es)

V 1.2



Integration Scale

- According to the number of transistors (or logic gates) integrated into an integrated circuit, devices are classified into the following categories:
  - SSI (small-scale integration): 3 – 30
  - MSI (medium-scale integration: 30 – 300
  - LSI (large-scale integration): 300 – 3,000
  - VLSI (very large-scale integration) > 3,000
  - ULSI (ultra large-scale integration) > 1,000,000



- Lithographic resolution (minimum feature size) has improved in parallel:
  - Submicron technology: $L_{min} \geq 0{,}35\mu m$
  - Deep-submicron technology: $0{,}1\mu m \leq L_{min} \leq 0{,}35\mu m$
  - Ultra-deep-submicron technology: $L_{min} \leq 0{,}1\mu m$

Key Parameters

- Supply Voltage.
- Logic Levels.
- Noise Margin.
- Current Ratings.
- Propagation Delay.
- Fan-Out.
- Power Dissipation.
- Speed–Power Product.

Supply Voltage

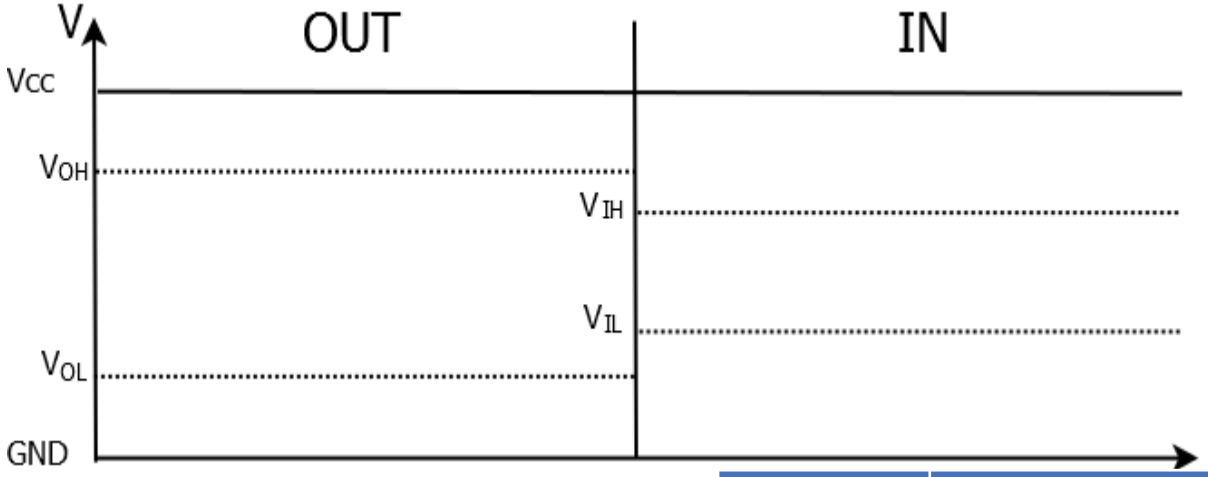
The supply voltage range that guarantees proper device operation.

Symbol	Parameter	Series	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V

If V_{CC} < Min., the device may not operate as specified.
If V_{CC} > Max. he device may be permanently damaged.
If Min. < V_{CC} < Max., he manufacturer guarantees proper operation.

Logic Levels

Logic levels define the voltage ranges corresponding to logic **'0'** and logic **'1'**. Rather than fixed values, these levels are specified as voltage ranges. They depend on the supply voltage, particularly in **CMOS** logic families, which support a wide operating voltage range.



V_{iH}: Minimum input voltage recognized as a logic HIGH.

V_{iL}: Maximum input voltage recognized as a logic LOW.

V_{oH}: Minimum output voltage for a logic HIGH.

V_{oL}: Maximum output voltage for a logic LOW.

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{iH}	Input High Voltage	2.0			V
V_{iL}	Input Low Voltage			0.8	V
V_{oH}	Output High Voltage	2.7	3.5		V
V_{oL}	Output Low Voltage		0,25	0.4	V

When two devices operate with different logic voltage levels, their inputs and outputs may be incompatible. This may result in improper operation (if the input threshold is not reached) or even damage the device (if the maximum allowable voltage is exceeded).

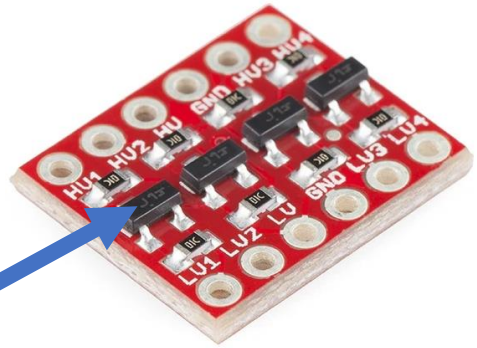
A common example is connecting a sensor to a microcontroller or microprocessor, since each device may operate at different logic voltage levels:

Arduino = 5V Raspberry/ESP = 3.3V

SOLUTION → Use a logic level translator (Level Shifter)

It may be **unidirectional** or **bidirectional**

<u>Example</u>: BSS138 (bidirectional 3.3V <-> 5V)

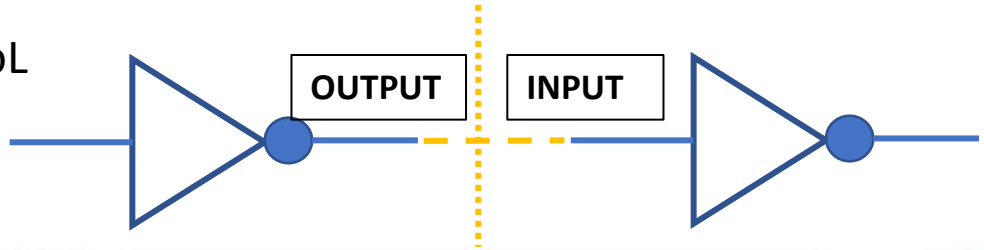


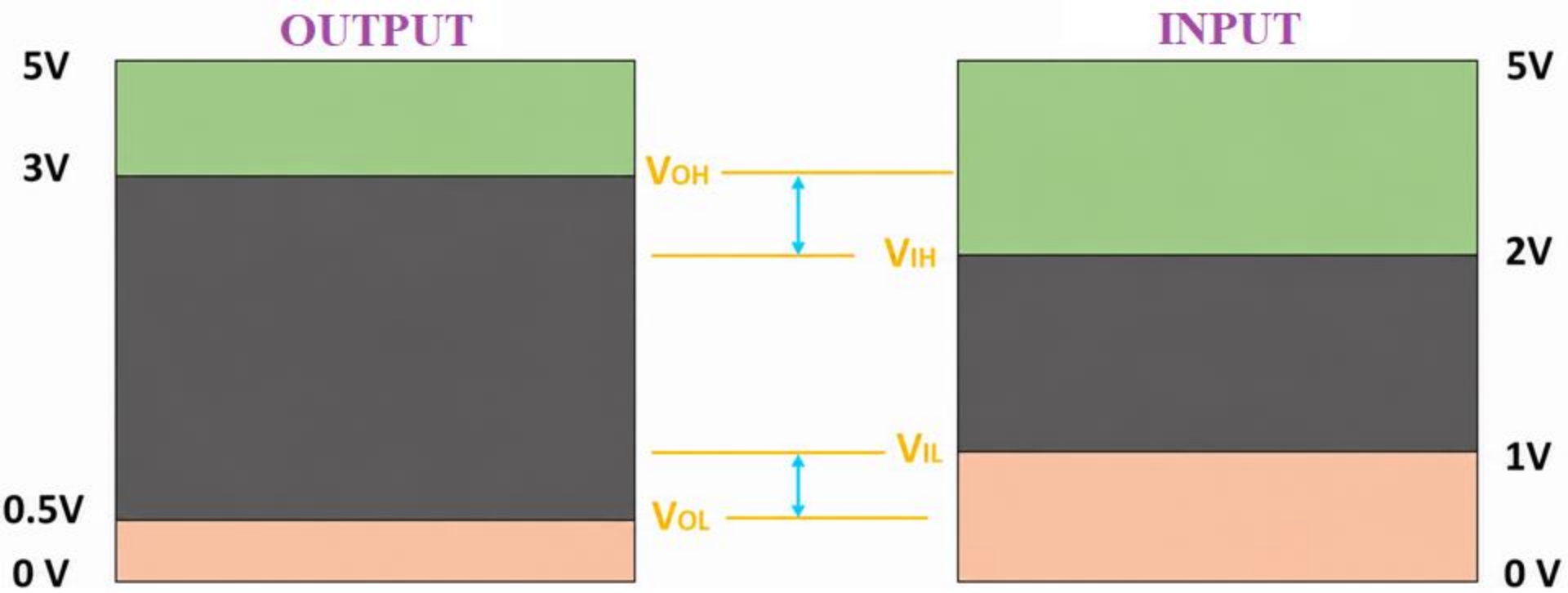
Noise Margin

$$V_{NH} = V_{oH} - V_{iH}$$

$$V_{NL} = V_{iL} - V_{oL}$$

Example using two inverters:





Current Ratings

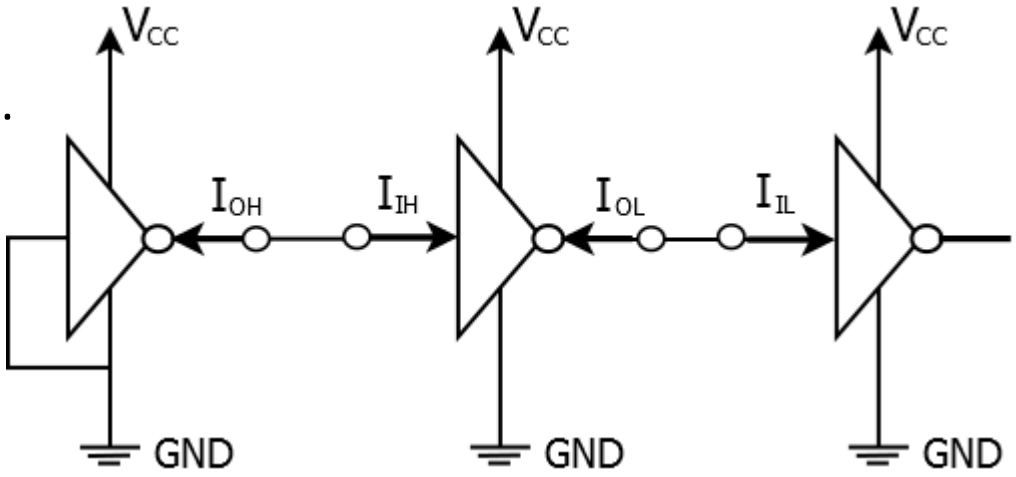
I_{iL}: Maximum LOW-level input current.

I_{iH}: Maximum HIGH-level input current.

I_{oL}: Maximum LOW-level output current.

I_{oH}: Maximum HIGH-level output current.

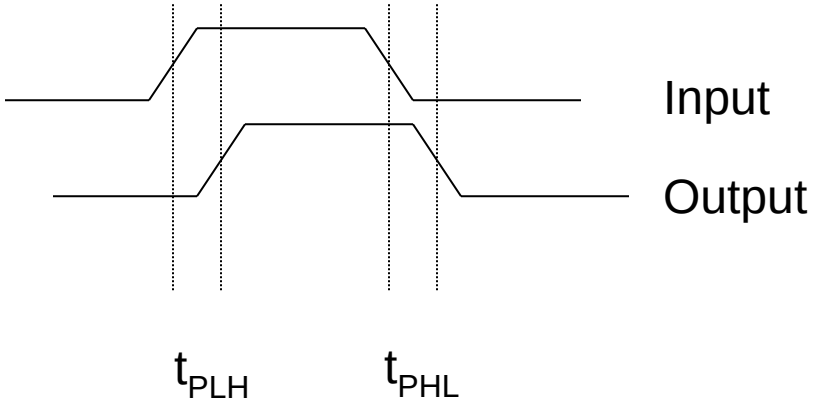
By convention, current flowing into the device is considered positive.



Parameter		Min	Nom	Max	Unit
I_{oH}: High Level Output current				-0.4	mA
I_{oL}: Low Level Output current				16	mA
	Test Conditions	**Min**	**Typ**	**Max**	
I_{iH}	V_{CC} = MAX V_I = 2.4 V			40	µA
I_{iL}	V_{CC} = MAX V_I = 0.4 V			-1.6	mA

Propagation Delay

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$



Parameter	From (Input)	To (Output)	Test Conditions	SN5404 SN7404			Unit
				Min	Typ	Max	
t_{PLH}	A	Y	R_L =400Ω C_L = 15pF		12	22	ns
t_{PHL}					8	15	

Fan-out: Maximum number of equivalent logic inputs that can be driven by a single output.

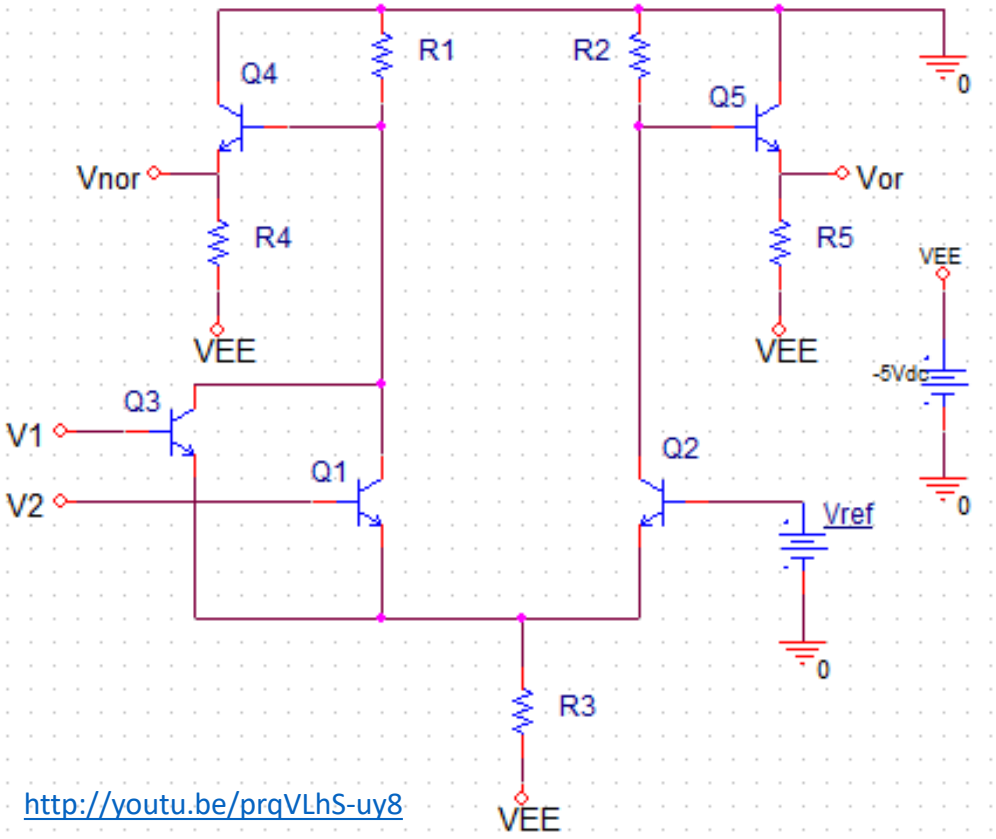
Power Dissipation: Average power consumption under both HIGH and LOW logic states.

Speed–Power Product: The product of power dissipation (mW) and propagation delay (ns), expressed in picojoules (pJ). It is a useful figure of merit for applications requiring a balance between speed and power consumption..

Technologies (I)

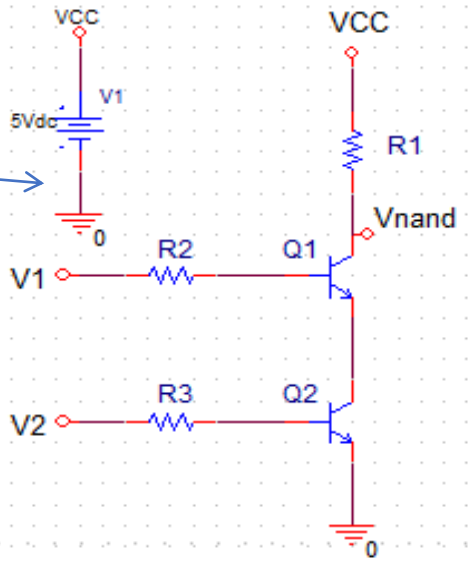
Bipolar Logic Families

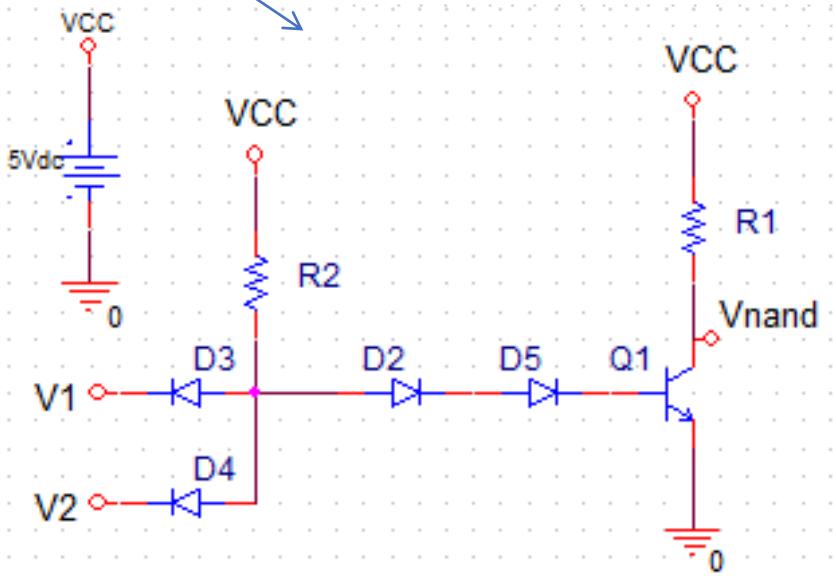
- RTL
- DTL
- TTL
- ECL



http://youtu.be/prqVLhS-uy8

http://youtu.be/Sxh4Vqe0sB4



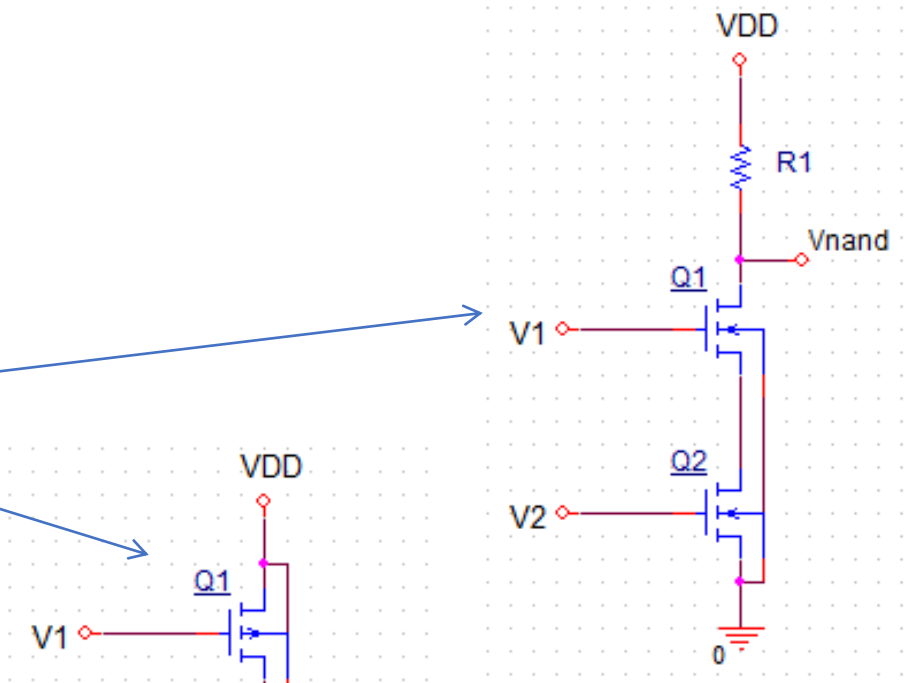


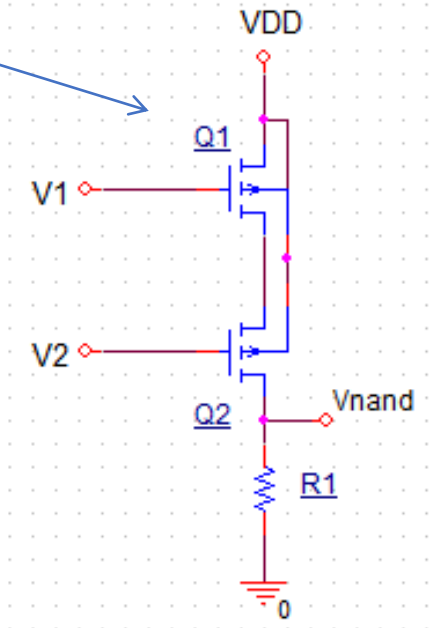
http://youtu.be/_taAQ-viwRE

Technologies (II)

MOS Logic Families

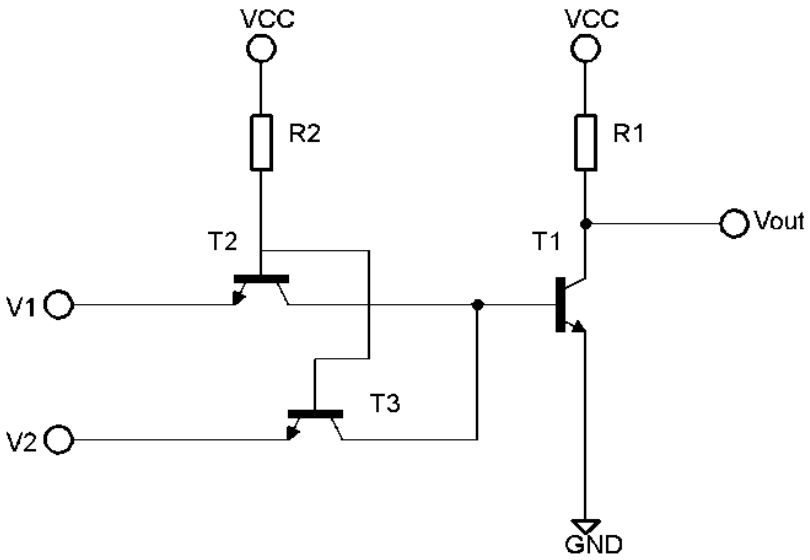
- NMOS
- PMOS
- CMOS



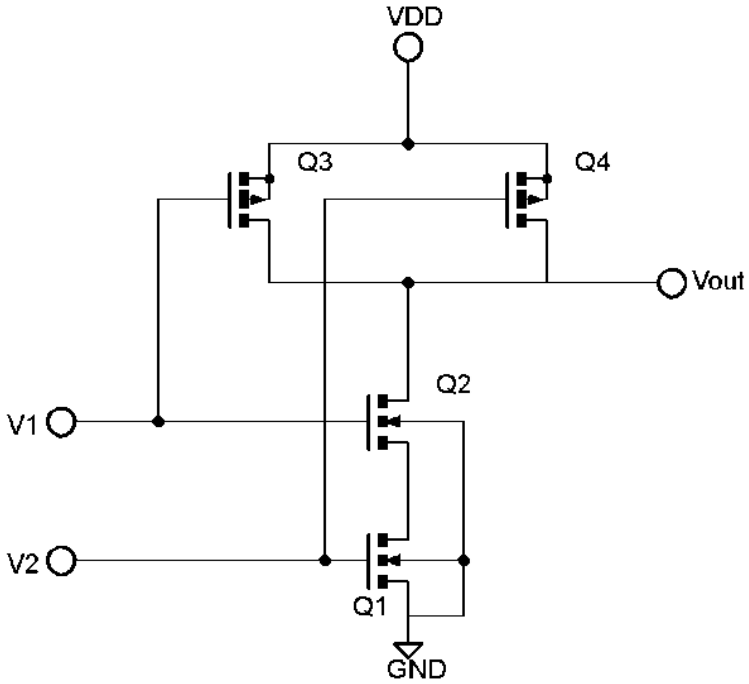


TTL & CMOS

TTL NAND



CMOS NAND



http://youtu.be/NHX-l-yHtDE

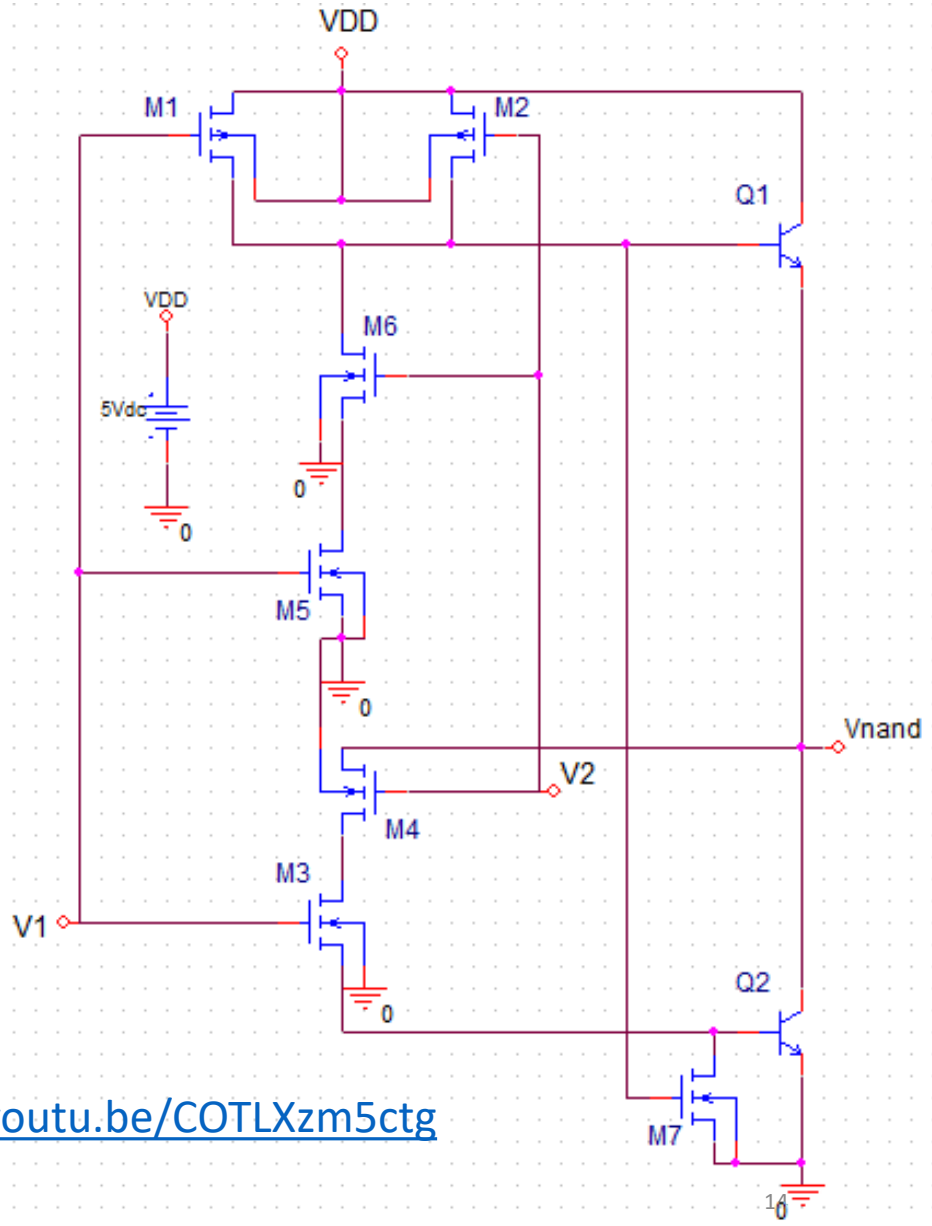
http://youtu.be/mnLFGk-tUtg

BiCMOS

Combines:

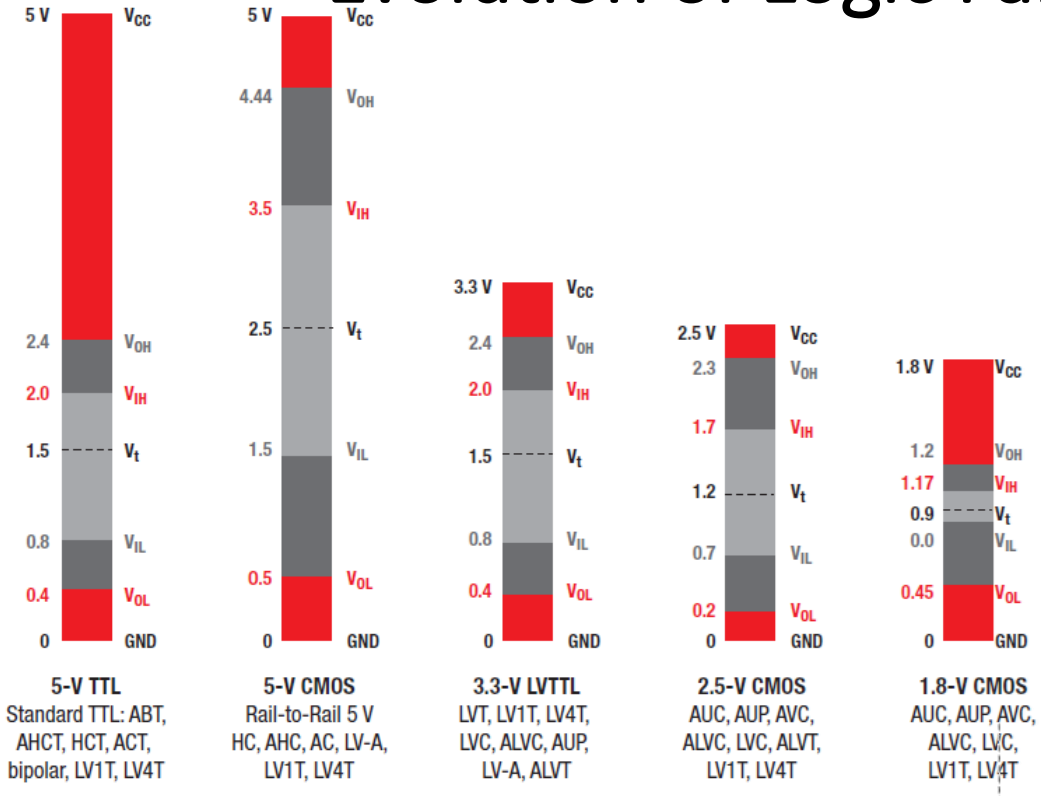
- The high switching speed of bipolar output transistors.
- The low power dissipation of CMOS technology.

The increased performance comes at the expense of greater circuit complexity.



http://youtu.be/COTLXzm5ctg

Evolution of Logic Families (I)



5-V TTL
Standard TTL: ABT, AHCT, HCT, ACT, bipolar, LV1T, LV4T

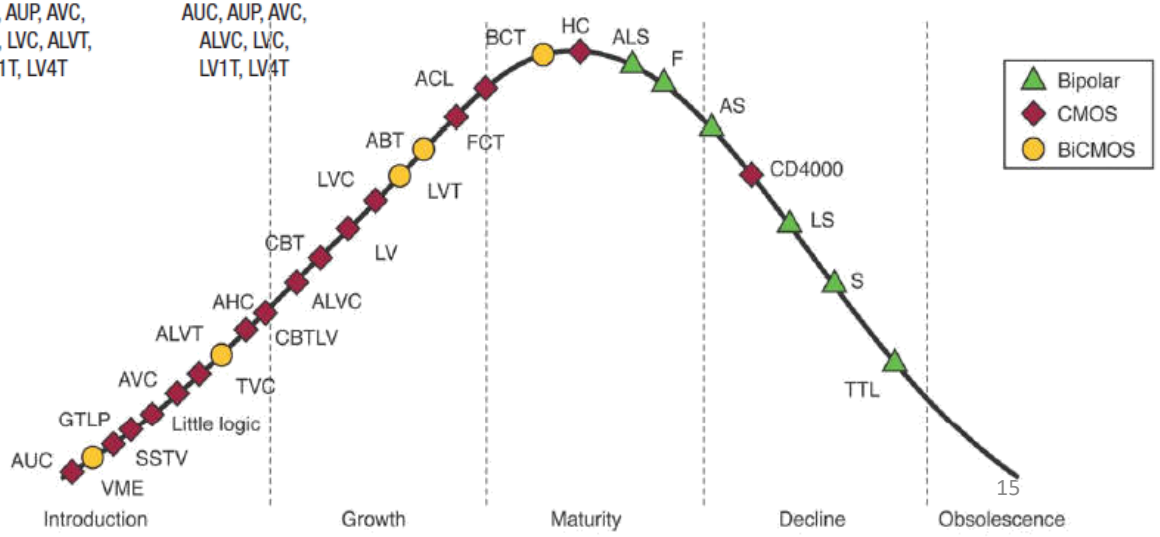
5-V CMOS
Rail-to-Rail 5 V HC, AHC, AC, LV-A, LV1T, LV4T

3.3-V LVTTL
LVT, LV1T, LV4T, LVC, ALVC, AUP, LV-A, ALVT

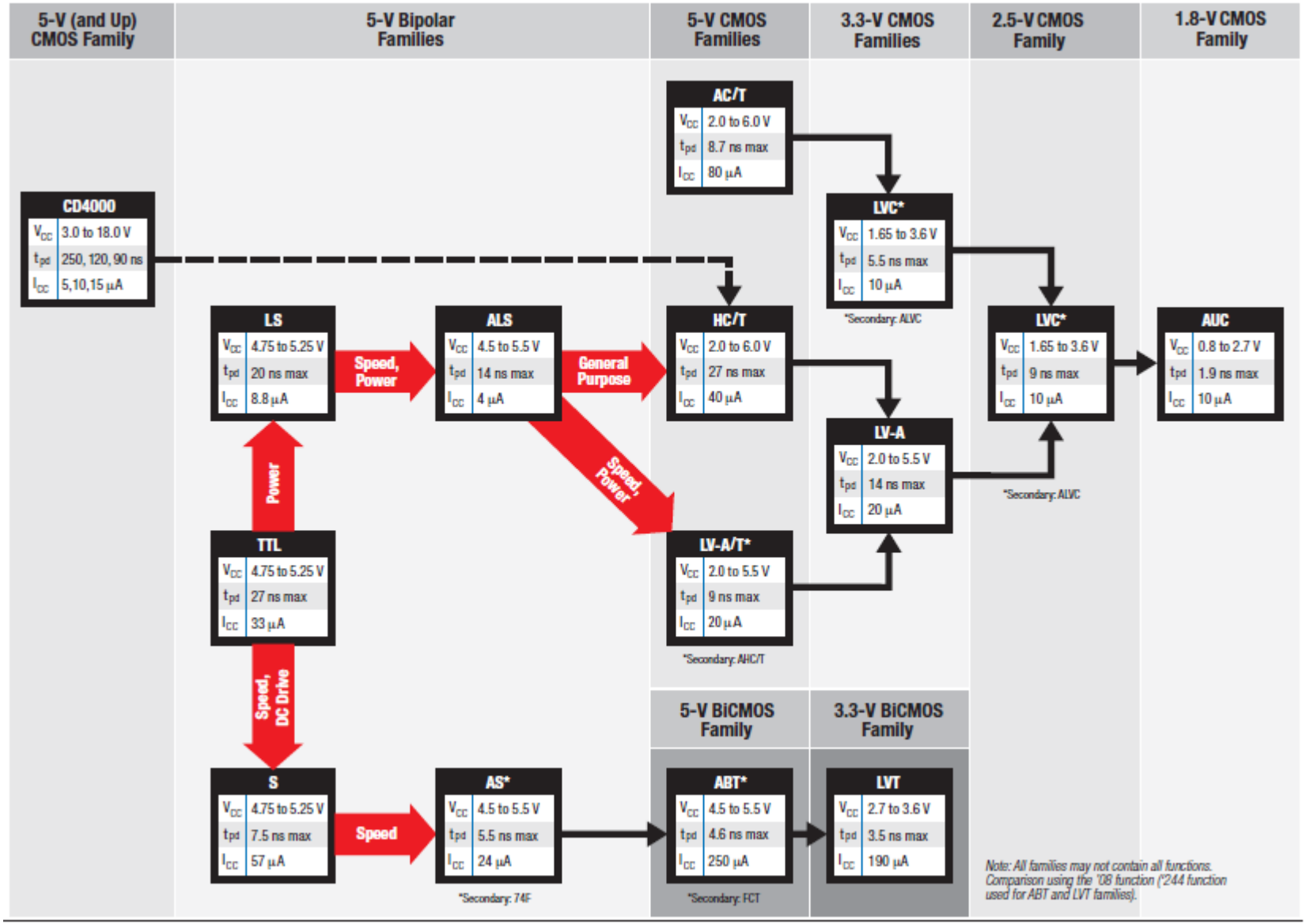
2.5-V CMOS
AUC, AUP, AVC, ALVC, LVC, ALVT, LV1T, LV4T

1.8-V CMOS
AUC, AUP, AVC, ALVC, LVC, LV1T, LV4T

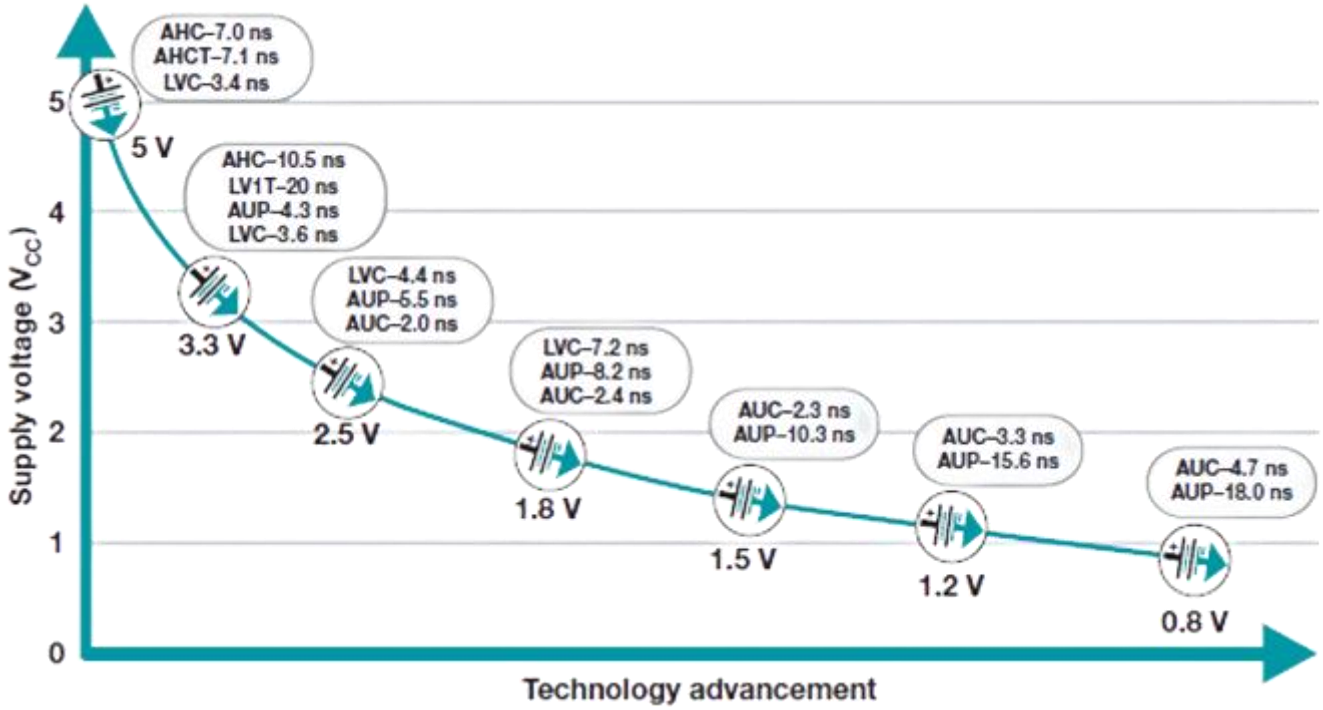
Texas Instruments Logic Guide 2014



Evolution of Logic Families (II)



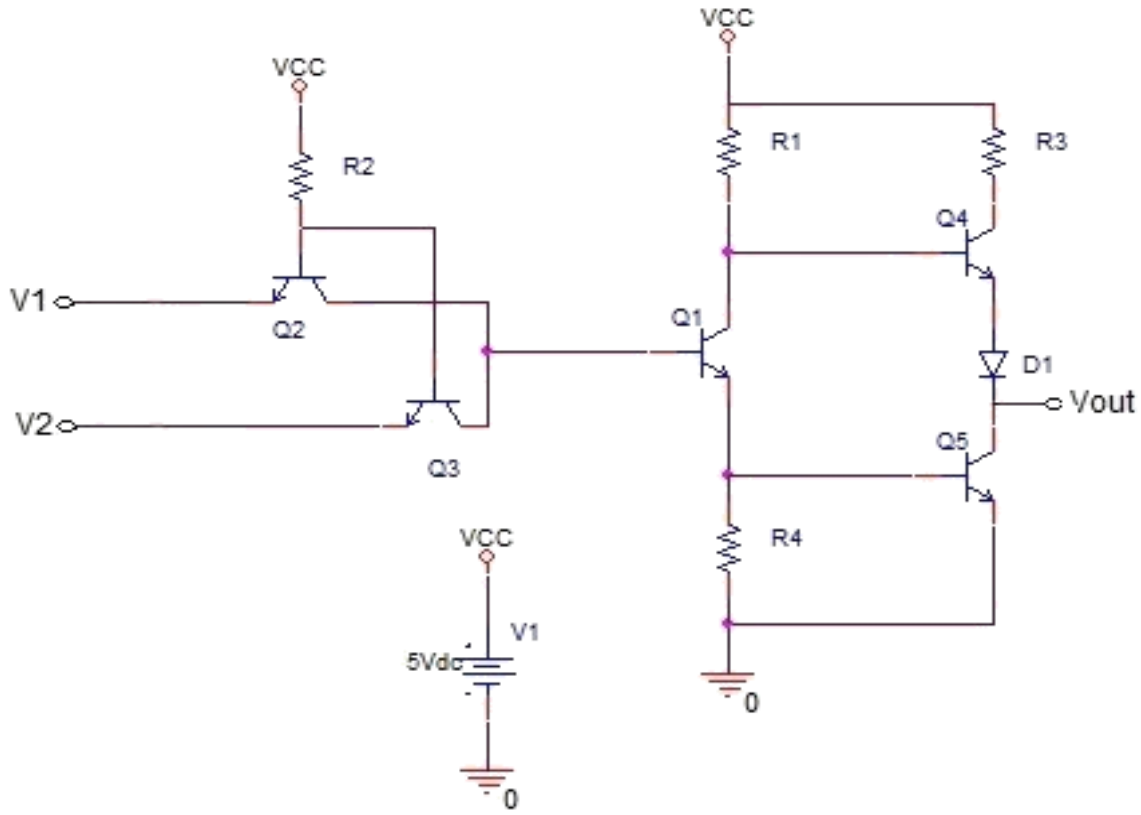
Evolution of Logic Families (I)



Texas Instruments Little Logic Guide 2018

Output Stages (I)

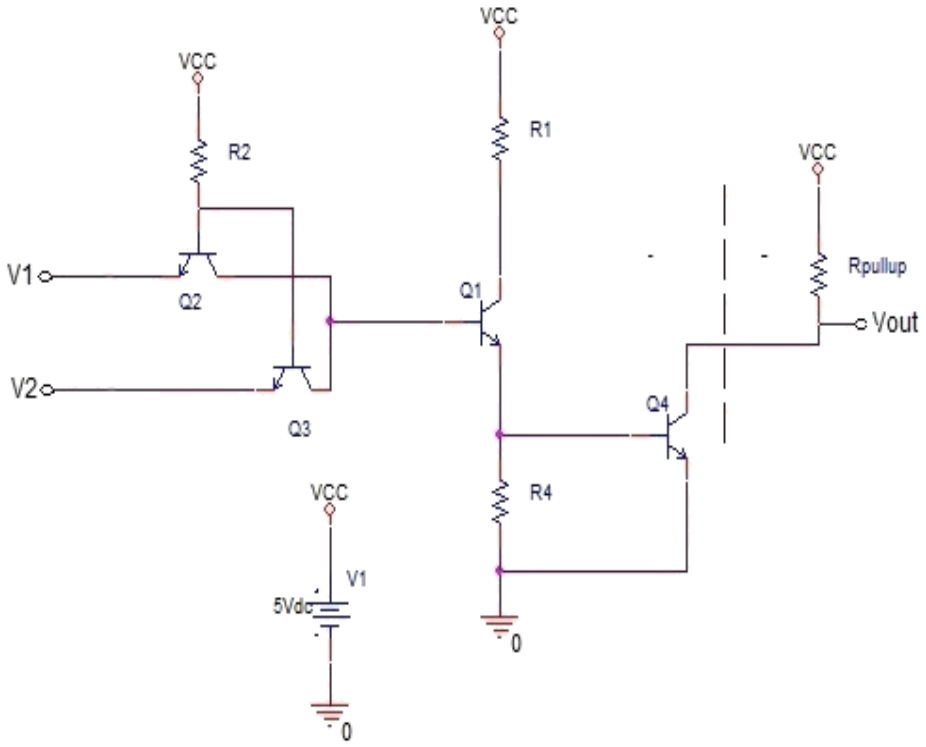
Totem-Pole Output: Default output stage



http://youtu.be/WqRMhfSYl1I

Output Stages (II)

Open-Collector / Open-Drain Output

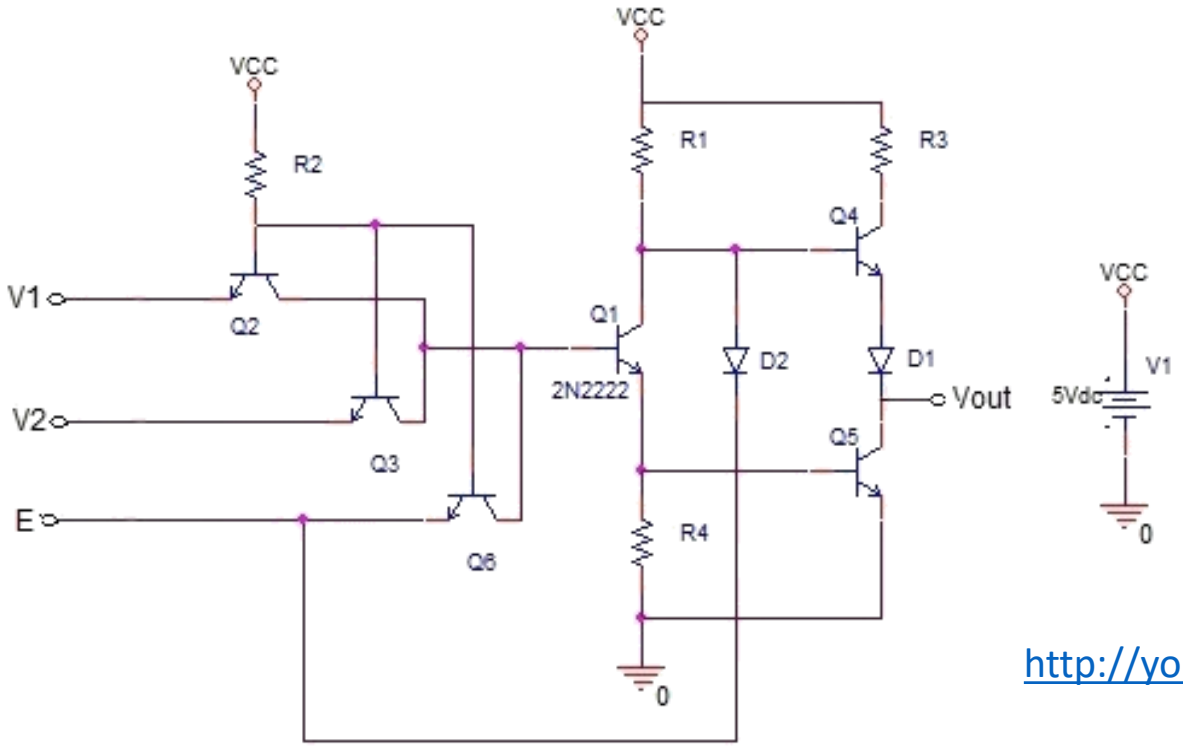


http://youtu.be/eIRzfj2IX_E

Requires an external pull-up resistor.
Supports wired-OR configurations.

Output Stages (III)

Three-State Output (Tri-State)



http://youtu.be/iwjR9Kzt0cM

Includes an enable input.
Allows the output to be disconnected by placing it in a high-impedance state.

References

- Texas Instruments Logic Guide: www.ti.com/logic