Logic families

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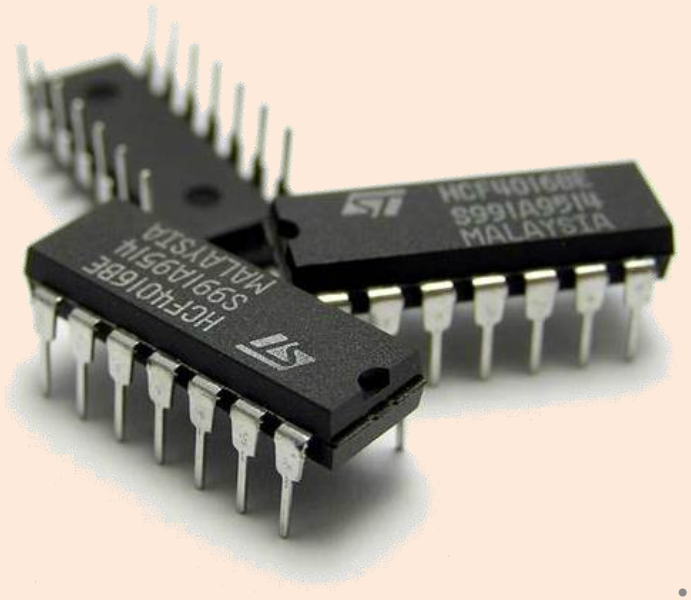
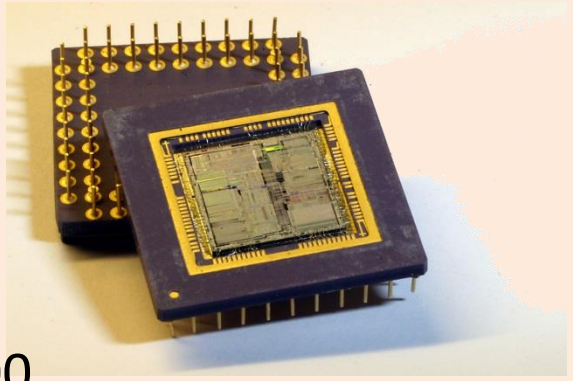
V 1.0



Scale of integration

- According to the number of transistors (or logic gates) inside, integrated circuits split in several categories:
  - SSI (short scale integration): 3 – 30
  - MSI (medium scale integration: 30 – 300
  - LSI (large scale integration): 300 – 3.000
  - VLSI (very large scale integration) > 3.000
  - ULSI (ultra large scale integration) > 1.000.000



- Resolution (minimum feature in lithography) has incremented gradually:
  - Submicron technology: $L_{min} \geq 0{,}35\mu m$
  - Deep submicron technology: $0{,}1\mu m \leq L_{min} \leq 0{,}35\mu m$
  - Ultra deep submicron technology: $L_{min} \leq 0{,}1\mu m$

Main parameters

- Supply voltage.
- Logic levels.
- Noise margin.
- Currents.
- Propagation delay.
- Fan-out.
- Power.
- Speed x power product.

Supply voltage

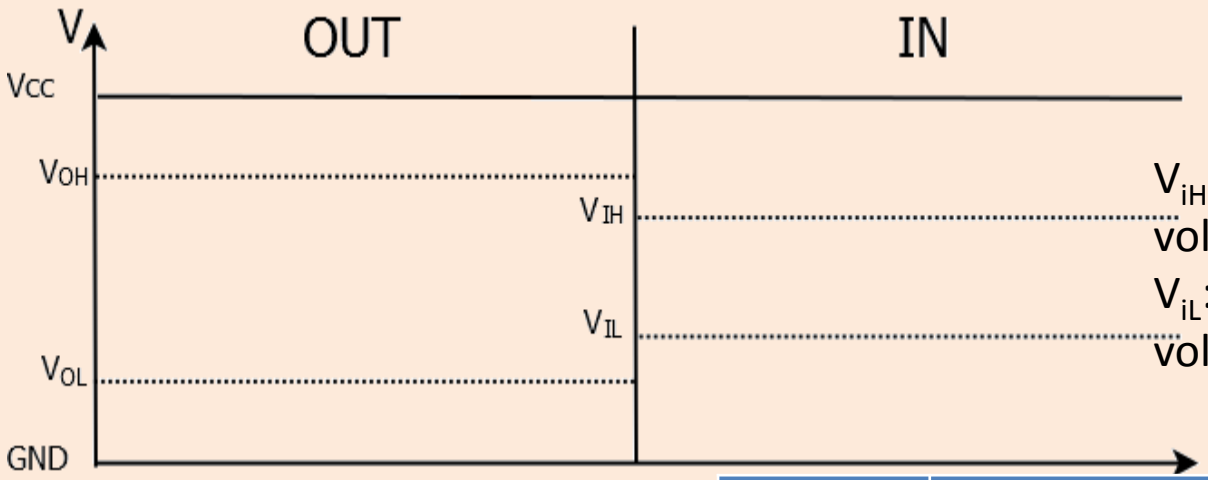
Supply voltage range that ensures the circuit functions properly.

Symbol	Parameter	Series	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V

If V_{CC} < Min. The device may not work as expected.
If V_{CC} > Max. the device may deteriorate.
If Min. < V_{CC} < Max. manufacturer guarantees proper performance.

Logic levels

Determine the voltage of logic “0” & “1”. These are not exact values but a range of them. Depend on supply voltage, especially in CMOS families that allow for a wide voltage span.



V_{iH}: minimum high level input voltage.

V_{iL}: maximum low level input voltage.

V_{oH}: minimum high level output voltage.

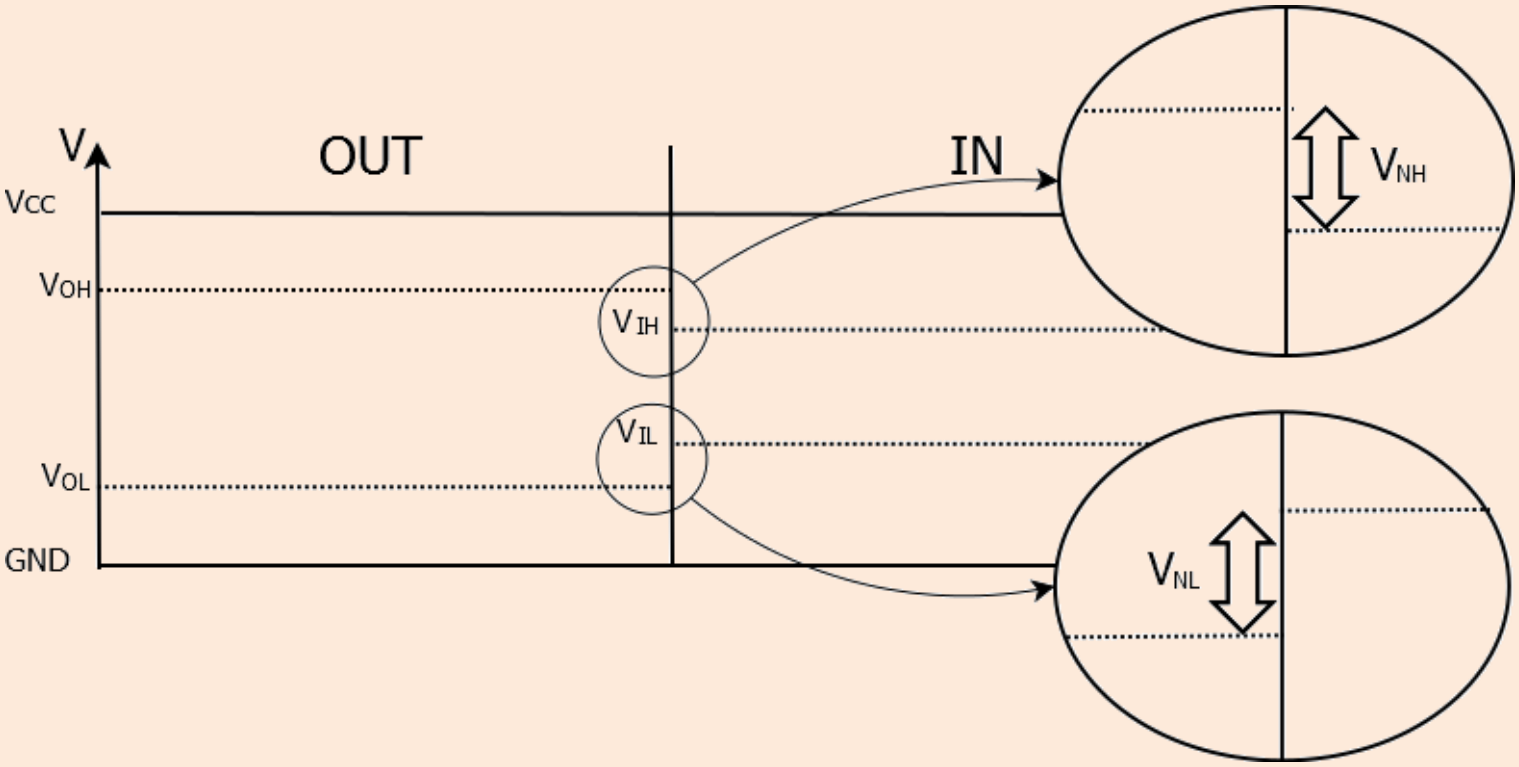
V_{oL}: maximum low level output voltage.

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{iH}	Input High Voltage	2.0			V
V_{iL}	Input Low Voltage			0.8	V
V_{oH}	Output High Voltage	2.7	3.5		V
V_{oL}	Output Low Voltage		0,25	0.4	V

Noise margin

$V_{NH} = V_{iH} - V_{oH}$

$V_{NL} = V_{iL} – V_{oL}$



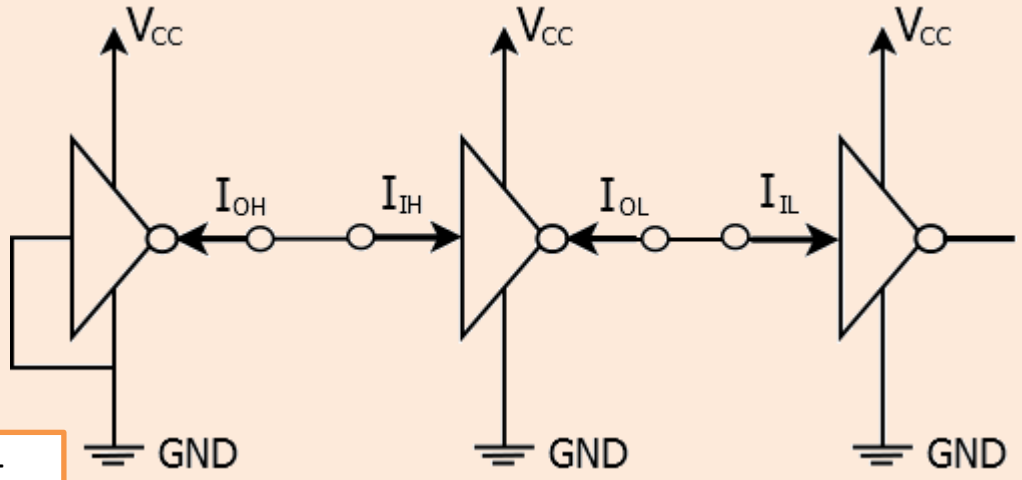
Currents

I_{iL}: maximum low level input current.

I_{iH}: maximum high level input current.

I_{oL}: maximum low level output current.

I_{oH}: maximum high level output current.

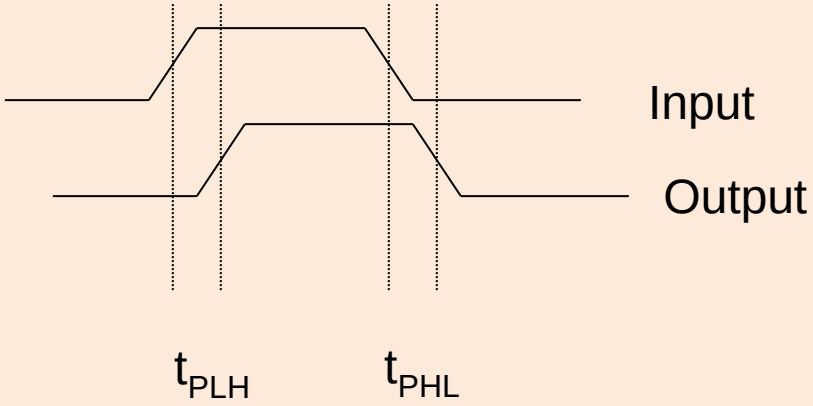


Currents are taken entering the IC by default.

Parameter		Min	Nom	Max	Unit
I_{oH}: High Level Output current					mA
I_{oL}: Low Level Output current					mA
	Test Conditions	**Min**	**Typ**	**Max**	
I_{iH}	V_{CC} = MAX V_I = 2.4 V			40	µA
I_{iL}	V_{CC} = MAX V_I = 2.4 V			-1.6	mA

Propagation delay

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$



Parameter	From (Input)	To (Output)	Test Conditions	SN5404 SN7404			Unit
				Min	Typ	Max	
t_{PLH}	A	Y	R_L =400Ω C_L = 15pF		12	22	ns
t_{PHL}					8	15	

Fan out: number of analogous circuits that can be connected to the output.

Power: average consumption at high and low level.

Speed-power product: power in mW by the propagation delay in ns. Result is pJ. It is a meaningful reference in applications where both speed and power are important.

Technologies

Bipolar technologies

- RTL
- DTL
- TTL
- ECL

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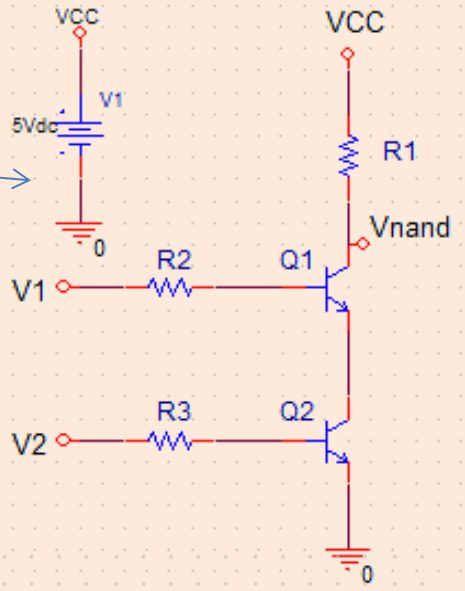

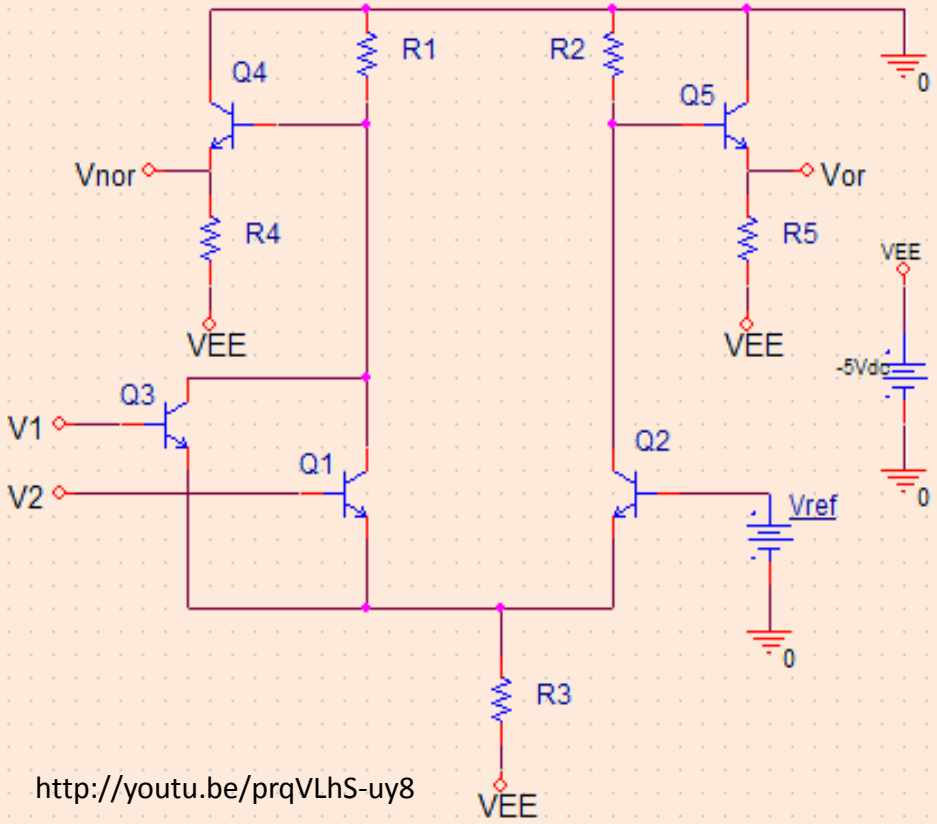

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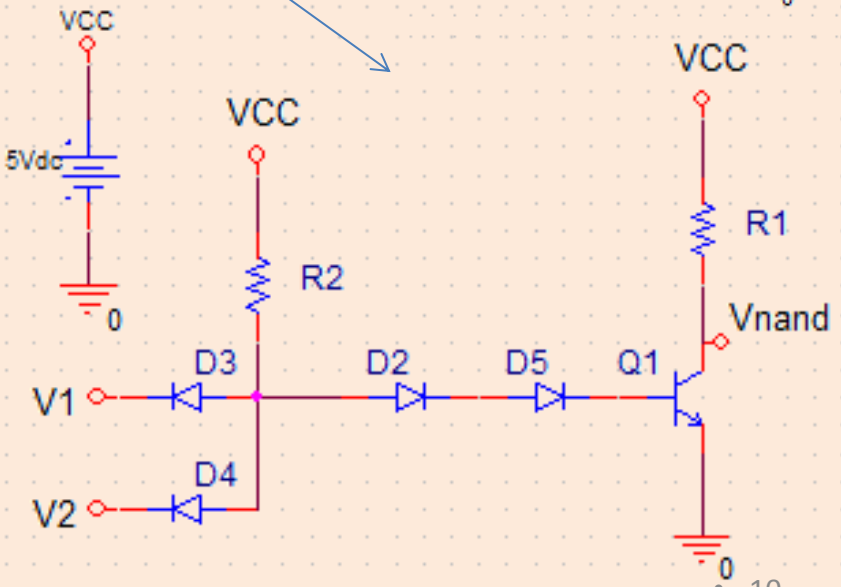

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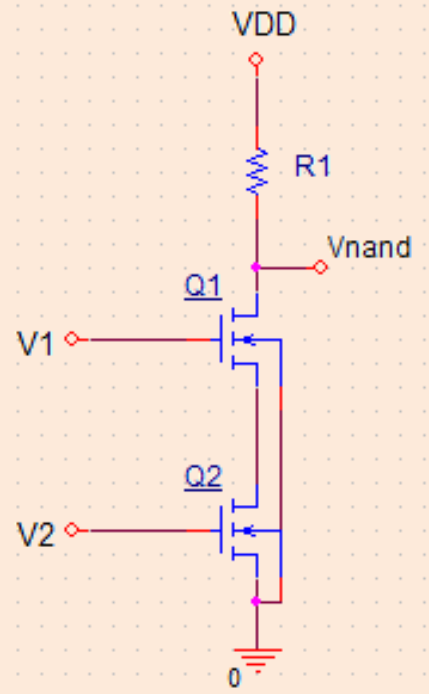
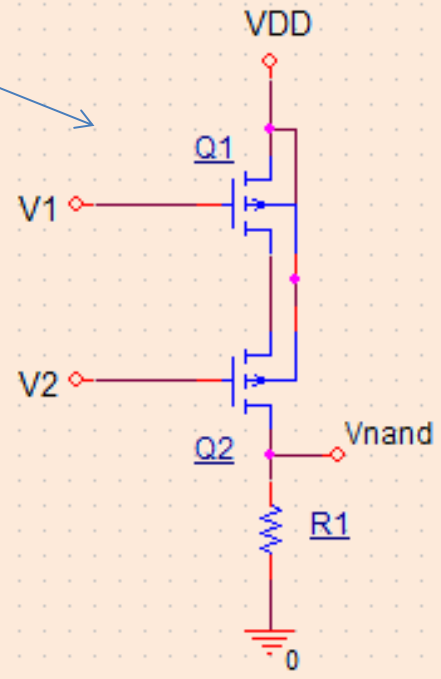
Technologies

MOS Technologies

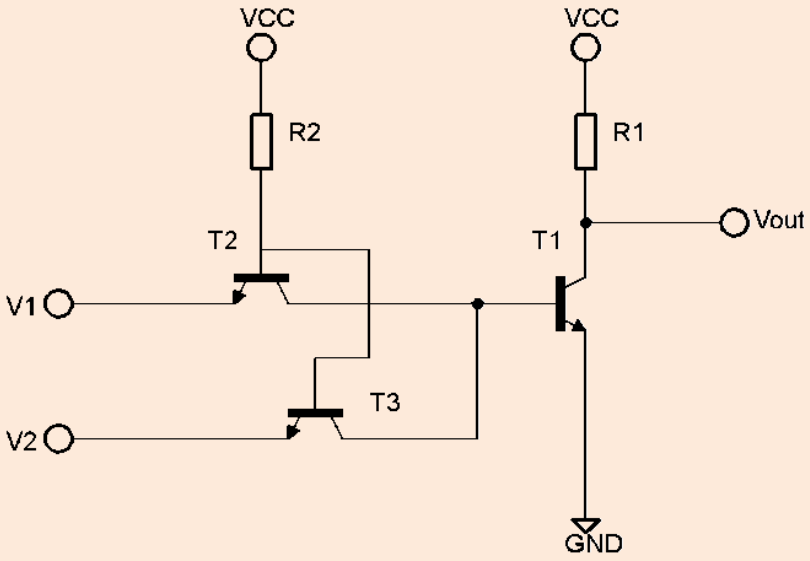
- NMOS
- PMOS
- CMOS





TTL & CMOS

TTL NAND



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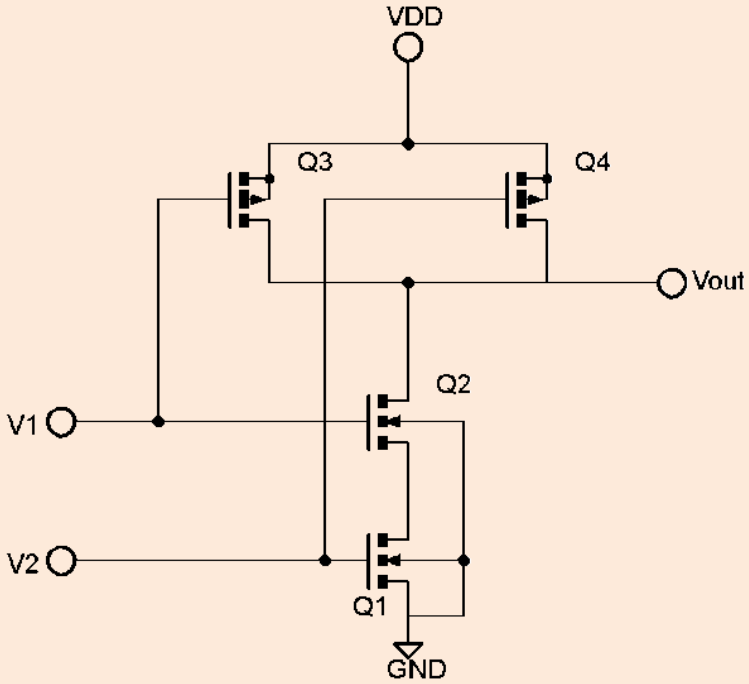
CMOS NAND



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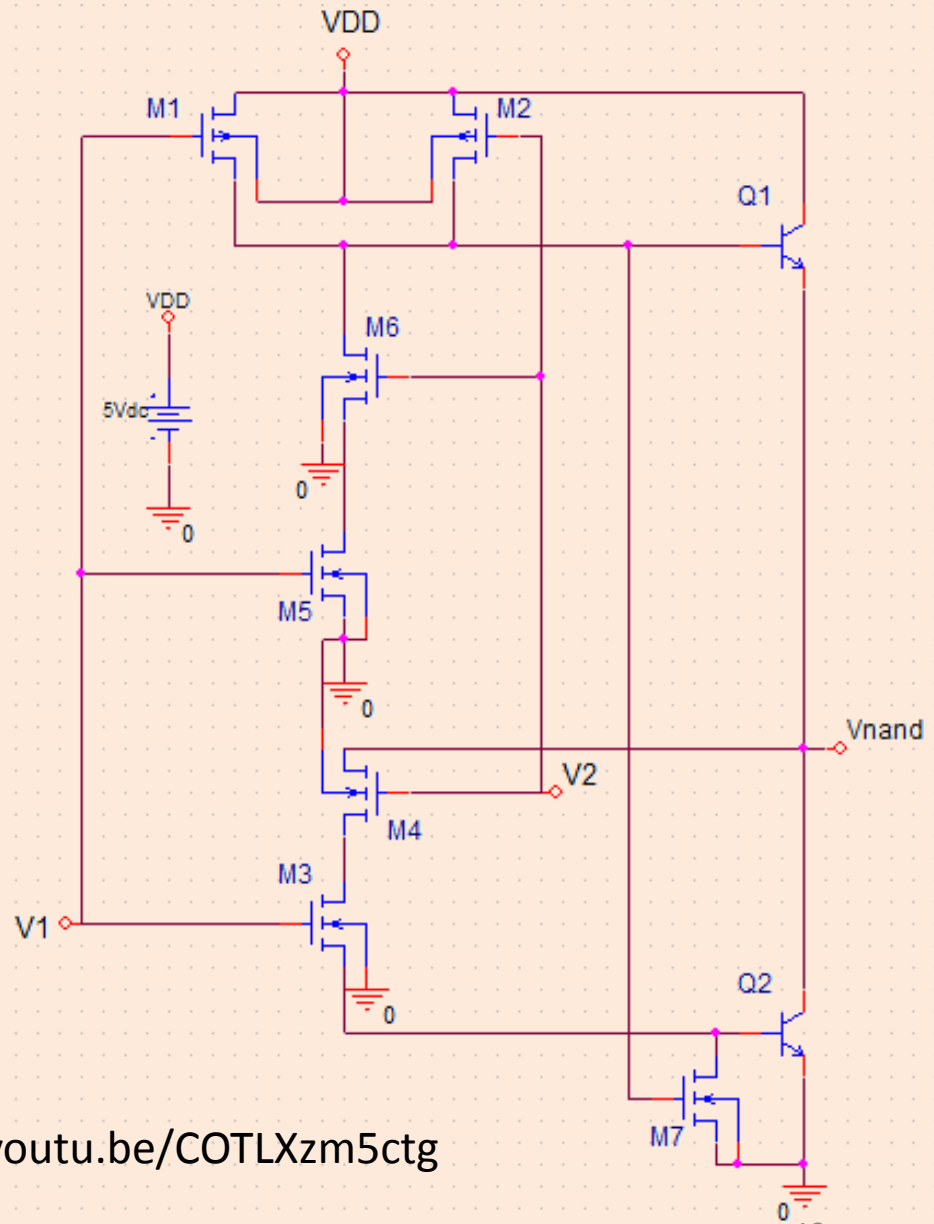
BiCMOS

Combines:

- The speed of bipolar transistors.
- Low dissipation of CMOS.

Introduces more complexity.



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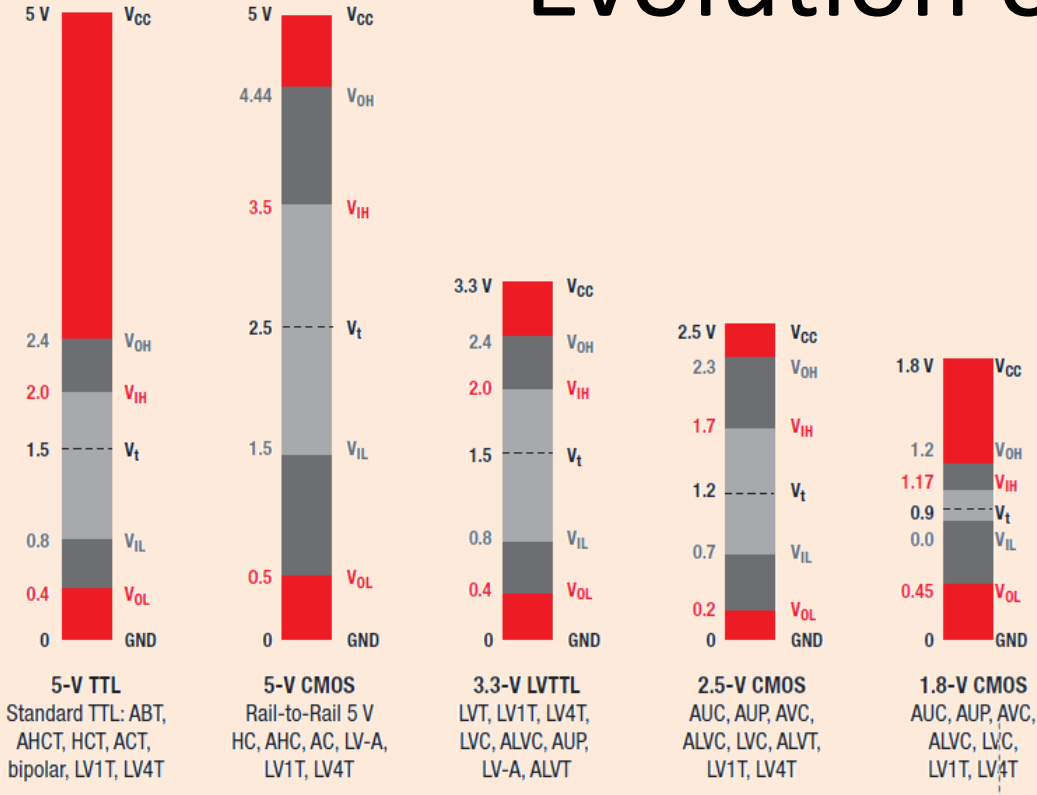
Evolution of logic families



5-V TTL
Standard TTL: ABT, AHCT, HCT, ACT, bipolar, LV1T, LV4T

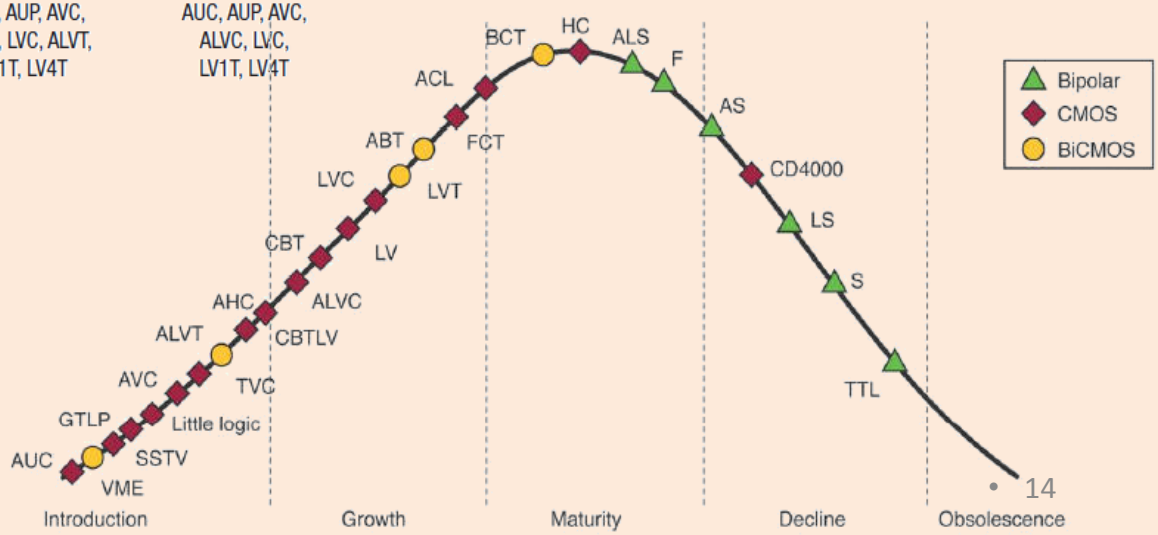
5-V CMOS
Rail-to-Rail 5 V HC, AHC, AC, LV-A, LV1T, LV4T

3.3-V LVTTL
LVT, LV1T, LV4T, LVC, ALVC, AUP, LV-A, ALVT

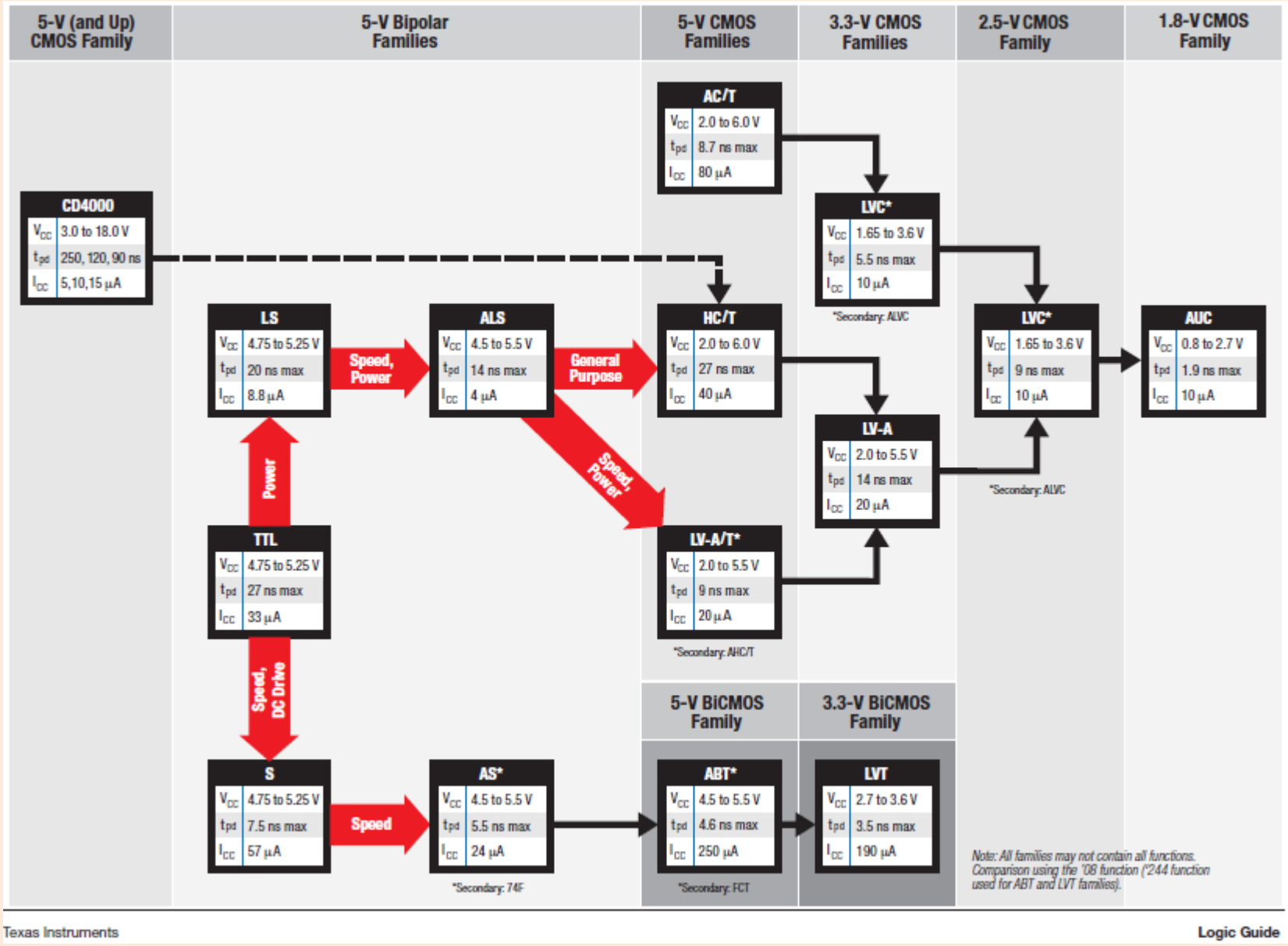
2.5-V CMOS
AUC, AUP, AVC, ALVC, LVC, ALVT, LV1T, LV4T

1.8-V CMOS
AUC, AUP, AVC, ALVC, LVC, LV1T, LV4T

Texas Instruments Logic Guide 2014

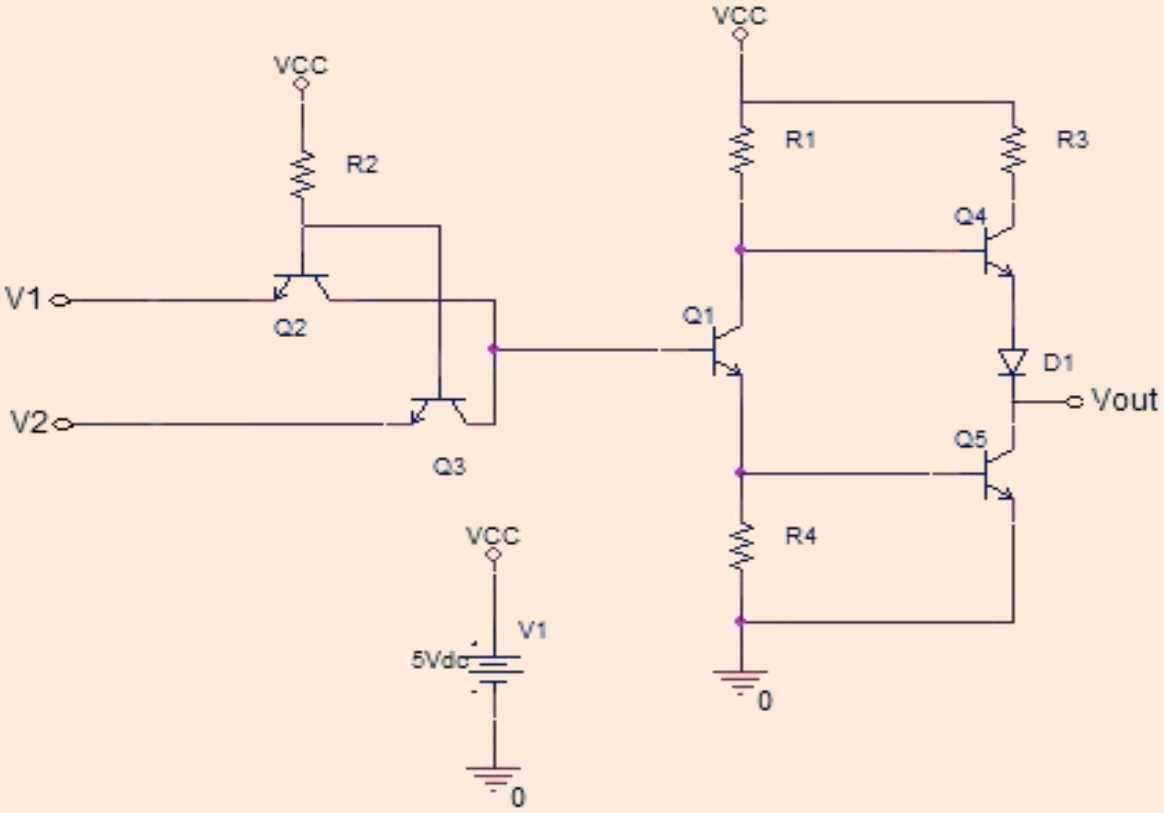


Evolution (II)



Output stages

Totem pole: default output stage



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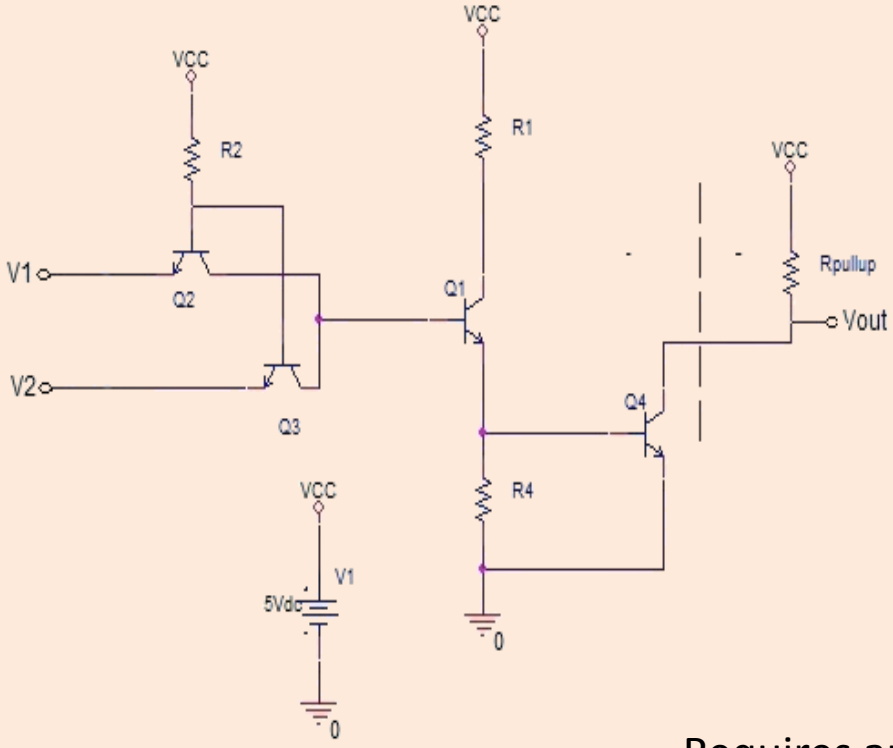
Output stages (II)

Open collector/drain



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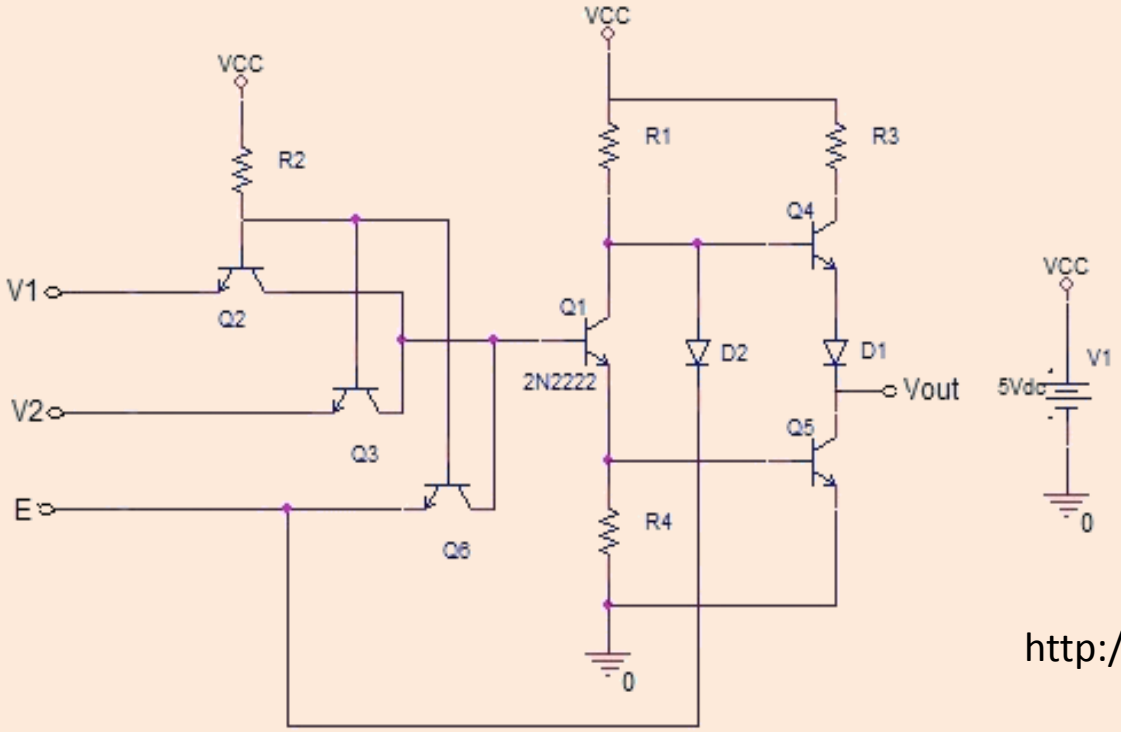
Requires an external pull-up resistor.
Makes OR-wired configuration possible.

Output stages (III)

Tri-state



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Provides an enable input.
Makes switching off (at high impedance) the output possible.

References

- http://diranieh.com/Electrenicas/DigitalAnalog.htm
- http://people.seas.harvard.edu/~jones/es154/lectures/lecture_7/lecture_7.html
- Texas Instruments Logic Guide: www.ti.com/logic