

Technology of Electronic Systems Laboratory Guide

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Introduction	5
Academic year 2015 / 2016	5
ACTIVITY 0	6
OBJETIVES	
REGULATIONS AFFECTING THE LABORATORY COURSE.	6
LABORATORY EXERCISES. SAFETY REGULATIONS AND ACCIDENT PREVENTION.	7
INSTRUCTIONS FOR THE ELABORACIÓN OF THE ACTIVITY REPORT:	9
ACTIVITY 1	10
OBJETIVES	10
EXERCISES	10
	11
ANALOG AND DIGITAL COMPONENTS	11
ACTIVE AND PASIVE COMPONENTS	11
PASSIVE COMPONENTS	11
PRACTICAL EXERCISE	23
INSTRUCTIONS FOR THE ELABORACIÓN OF THE EXERCISE REPORT:	23
ACTIVITY 2	24
OBJETIVES	24
EXERCISES	24
	25
CLASIFICACIÓN	25
DISCRETE SEMICONDUCTORS	25
INTEGRATED SEMICONDUCTORS	30
NON-ELECTRONIC COMPONENTS	31
PRACTICAL EXERCISE	33
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT:	33
ACTIVITY 3	34
OBJETIVES	34
EXERCISES	34
	35
Manual design	36
Computer assisted	36
MANUAL DESIGN	37
PRACTICAL DESIGN	38

PRÁCTICAL EXERCISE	39
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT	39
ACTIVITY 4	41
OBJETIVES	41
EXERCISES	41
FILE GENERATION	42
ACTIVITY 5	45
OBJETIVES	45
EXERCISES	45
	46
LAYOUT PROJECT CREATION	46
CONFIGURATION PARAMETERS	47
PLACING THE COMPONENTS	51
MANUAL ROUTING	51
FINISHING THE DESIGN	52
PRINTING	55
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT	56
ACTIVITY 6	57
OBJETIVES	57
EXERCISES	57
	58
COMPONENT AUTO PLACEMENT	58
AUTO ROUTING	58
DOCUMENTATION	59
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT	61
ACTIVITY 7	62
OBJETIVES	62
EXERCISES	62
	63
PCB POST PROCESSOR	63
DOCUMENTATION DELIVERY	65
INSTRUCTIONS FOR THE ELABORATION OF THE ACTIVITY REPORT	65
ACTIVITY 8	66
OBJETIVES	66

EXERCISES	66
	67
PHOTO PROCESS	67
CHEMICAL ETCHING	68
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT	69
ACTIVITY 9	70
OBJETIVES	70
ACTIVITIES	70
	71
FINAL PROCESS	71
INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT	73

4

Introduction

Academic year 2015 / 2016

This document contains handouts for the use of students registered for the Technology of Electronic Systems course in its laboratory part. This course is part of the degree on Industrial Electronics and Automation Engineering, located on the first semester of the third year.

ACTIVITY 0

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB INTRODUCTORY ACTIVITY

OBJETIVES

- > Presentation and Regulations for the Technology of Electronic Systems Lab.
- > To get to know the facilities where the lab course takes place.
- \blacktriangleright To learn the potential risks connected with the use of the facilities.

REGULATIONS AFFECTING THE LABORATORY COURSE.

The regulations affecting the lab course are included in the general regulations of the course which refers to the lab as follows:

- a) The command of the practical part of the subject will be evaluated individually. For this purpose the reports submitted by the students along the course along with the result of a practical test at its end will be taken into account. The structure and contents the reports are expected to include will be explained for each exercise.
- b) In order to pass the subject, both the theoretical part and the lab one will have to be successfully passed. In that case, the final mark will result from the arithmetic mean of both individual marks.

LABORATORY EXERCISES. SAFETY REGULATIONS AND ACCIDENT PREVENTION.

As in every university lab, some rules have to be followed in order to guarantee the integrity the following aspects:

- Firstly, personal safety.
- Optimal academic performance.
- Avoid unintended damage on the use of instrumentation and components.
- Order and classification of components.

Unawareness of potential dangers or negligence may result in different types of accidents, some of which may have serious consequences.

Most common accidents at the electronics laboratory.

Among the most common accidents in the electronic technology lab, we can sort:

- Electric shock.
- Skin burns due to either manual soldering procedures or handling of chemicals (printed circuit board manufacturing).
- Wounds caused by the use of tools (scissors, pliers, etc.).

Effects of electric current on the human body.

Electric energy, in the form of electric current, when traversing the human body causes a number of disorders as a result of its interaction with organs. Their nature and intensity depend on the following factors:

• Current's intensity

From 0 to 10 mA: Muscle reflex movements (cramps).

From 10 to 25 mA: Muscle spasms, tetanic contraction of arm and hand muscles refusing to release objects. Breathe difficulty. Blood pressure raise.

From 25 to 30 mA: Heart arrhythmia. Strong tetanic contraction. Breathe muscles are affected and, after 4 seconds, suffocation symptoms and electric burns appear.

From 40 mA to 10 A: Heart ventricular fibrillation.

More than 10 A: Heart arrest. If the current circulation doesn't last long (less tan a minute) the heart may resume normal operation since the current behaves both as a fibrillating and defibrillating agent.

Skin burns are caused by the current's thermal effect.

• Contact duration

It is determining mainly when the current is higher than 30 mA.

• Influence of voltage and resistance on the organism

The influence of voltage is due to the current circulation it produces according to the Ohm's law.

The skin isolates the human body and opposes certain electric resistances to current circulation since its tissues are poor conductors. These tissues can be better compared to a capacitor.

Against direct current, the skin opposes a higher resistance than against alternate current. The effects of direct current are, therefore less serious than those caused by alternate current by a ratio of one to four approximately.

A rough and dry skin may have an electric resistance of around 50.000 Ω . However, a soft and wet skin may have roughly 1.000 Ω .

Voltages considered as low, 220 V and 380 V, may then produce electrocution.

• Other factors that influence the consequences of electric shock are:

- Resistance of the body between the contact places.
- Course of the current inside the body.
- Current frequency.

First aids.

• Accidents caused by chemicals

They may take place when working on printed circuit board manufacturing. These processes entail the handling of chemicals in trays. If a corrosive chemical splashes in the eyes, proceed immediately to wash them with abundant water. If splashes are on the skin, wash it likewise.

• Electric shock

When the voltage is high and the victim is still in touch with the current source, he or she must be released:

- Turn off power first.
- Detach the victim from the source. To do this, isolate yourself from ground to avoid receiving the shock.

In case the victim has lost consciousness but not breathe, the skin hasn't changed color, heart beats are present and pupil is normal in size, it is enough to place the victim in lateral position, watching breathe and awaiting the arrival of medical assistance.

In case the victim has lost consciousness and breath assisted breathing must be applied. If no heartbeat is perceived, pupils are dilated and the skin is pale, a heart massage must accompany the assisted breathing.

Prevention.

When cables have to be handled, power must be turned off first. Before restoring power supply go over all connections to make sure they are all correctly wired.

All checks and measures will be carried out with isolated probes.

No steams coming from chemicals must be inhaled.

It is necessary to check polarity of components before connecting them, especially for electrolytic capacitors.

INSTRUCTIONS FOR THE ELABORACIÓN OF THE ACTIVITY REPORT:

No report is required for this exercise.

ACTIVITY 1

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PASSIVE ELECTRONIC COMPONENTS

OBJETIVES

- > Study the different types of passive electronic components.
- ➤ Classify them.
- Identification of components in the lab.

EXERCISES

- 1. Resistor identification and measuring.
- 2. Resistor tolerance check.
- 3. Capacitor identification and measuring.
- 4. Inductance measuring.
- 5. LDR test.

INTRODUCTION

One major goal of this activity is to enforce student's awareness on the numerous ways of classifying the elements used in electronic equipment.

We will classify component according to several aspects that differentiate them. We will also include some elements that, although not electronic, are frequently part of electronic equipment

As in any classification, there may be some aspects subject to discussion. We hope they will be clarified by the subsequent explanations.

Connection elements are numerous and diverse. We will postpone to the next activity devices such as cables, switches and connectors. Printed circuit boards are also considered connection elements.

ANALOG AND DIGITAL COMPONENTS

The first classification and therefore the most generic one would refer to the field where components are to be mainly used, that is analog or digital circuits. Nevertheless, numerous components are used in both types of circuits making this taxonomy not very adequate.

ACTIVE AND PASIVE COMPONENTS

We will focus on the classification of components according to their energetic balance:

- Active: these are components meant to transfer energy.
- Passive: the power absorbed is either stored or transformed into heat.

PASSIVE COMPONENTS

Classification of passive components according to their functionality:

Component type	Characteristic property
Resistor	Resistance
Capacitor	Capacity
Inductor	Magnetic induction

Resistors

Resistors are based on the resistance opposed by all conductors to the electric current flow. It is determined by material's resistivity (ρ) and its geometric characteristics.

Resistivity is conductivity's inverse, which in turn is given by electron mobility, their concentration and charge.

$$\rho = \frac{1}{\sigma} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V * se_{a}} \quad \sigma = \mu_{h} * n * e^{\mu_{h}} = \frac{m^{2}}{V *$$

If we assume that current's density is constant throughout conductor's cross-section (which is true for low and medium frequency):

$$R = \int \rho \frac{dx}{A}$$

If the material is homogeneous, its resistivity will be constant. If its cross-section is also constant we have:

$$R = \rho \frac{L}{A}$$

Technical specifications:

Nominal resistance: Rn resistance expected from the resistor. It corresponds to a normalized value. (at 25°C)

Tolerance: maximum difference between nominal and real value. It is given as a percentage and is also a normalized value.

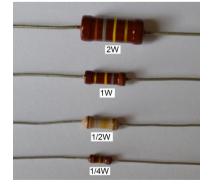
According to thee tolerance resistor are manufactured in series of normalized values.

Series	Tolerance	Sig	Significant digits of the nominal value																						
E6	±20 %	10				15				22				33				47				68			
E12	±10 %	10		12		15		18		22		27		33		39		47		56		68		82	
E24	±5 %	10	11	12	13	15	16	18	20	22	24	27	30	33	36	39	43	47	51	56	62	68	75	82	91

When a certain value exists in a series, all its multiples of ten will exist as well. If we have '22' for instance, we will also have from 0,22 Ohms $(22 \cdot 10^{-2})$, to 22 Mega-Ohms $(22 \cdot 10^{6})$.

Nominal power: amount of power that can be dissipated continuously without damage. There are also normalized values usually in powers of 2 steps.

Relative sizes of carbon resistors are depicted in the figure below.



Nominal voltage: it is determined by the nominal power and the nominal resistance. It cannot exceed the maximum working power. $V_n = \sqrt{P_n R}$

12

Maximum working voltage: maximum DC voltage that can be applied to the resistor. It cannot exceed the nominal voltage. The value that makes both equal is called *critical resistance*. Below this value of resistance, the nominal voltage is the limiting factor, whereas above it is the maximum working voltage what matters. For instance, for 1W resistors with a working voltage of 500V, both parameters are equal for a 22.36 ohms resistor. $500 = \sqrt{1R}$

Maximum overload voltage: maximum voltage that can be applied for a short period of time (5 seconds)

Nominal temperature: temperature for which the nominal voltage is given.

Voltage coefficient: unitary change in resistance with respect to the change in applied voltage.

$$\frac{\Delta R / R}{\Delta V}$$

Maximum temperature: maximum working temperature of the component. The dissipation curve determines a maximum temperature from which the available power is 0% of the nominal power.

Temperature coefficient: variation of the resistor's value as a result of the influence of temperature on resistivity. Only the first order term is usually taken into account:

R=R(1+*d*\$)

Frequency response: variation of the resistor's value as a result of the influence of frequency on current density.

Most resistors show their nominal value as a series of colored bands that can be interpreted as shown in the following table:

Activity:	1
-----------	---

	Color code of fixed resistors. IEC 60062 UNE-EN 60062										
		POW	VER RANG	GES FOR C.	ARBON F	ILM	RE	SIS	STORS 1/8, 1/	4, 1/2, 1, 2	W
3 ó 4 bands Series: E6-E12-E24					5	5 bar	All series				
	- (]	2° N	° ceros TOI	<u> </u>		- -]	2°	3	° Nº ceros Tol	 	$\begin{array}{c} \alpha \\ \text{Temperature} \\ \text{coefficient} \\ (10^{-6} \ ^{\circ}\text{C}) \end{array}$
Silver	-	-	10-2	$\pm 10\%$	Plata		-		10-2		
Gold	-	-	10-1	±5%	Oro		-		10-1		
Black	-	0	10^{0}		Negro	- () ()	10^{0}		±250
Brown	1	1	10 ¹	$\pm 1\%$	Marrón	1 1	. 1		10 ¹	±1%	±100
Red	2	2	10^{2}	$\pm 2\%$	Rojo	2 2	2 2		10^{2}	±2%	±50
Orange	3	3	10^{3}	-	Naranja	3 3	3 3	~	10^{3}	-	±15
Yellow	4	4	10 ⁴	-	Amarillo	b 4 4	4 4	ł	10^{4}	-	±25
Green	5	5	10 ⁵	±0,5%	Verde	5 5	5 5	~	10^{5}	±5%	±20
Blue	6	6	10^{6}	±0,25%	Azul	6 6	56	5	10^{6}	-	±10
Violet	7	7	-	±0,1%	Violeta	7 7	7	7	-	-	±5
Grey	8	8			Gris	8 8	8 8	\$	-	-	±1
White	9	9			Blanco	99) 9)	-	-	
None				± 20 %					-	±20%	
1° 2° Signific digits	ant		Factor	Tolerance	1°,2°,3° Significa	ant d	igit	S	Factor	Tolerance	Sixth band wider, dashed or spiral

Note: E48 series has a tolerance of 2% and E96 1%.

Classification:

		Combon	Compositon			
	Fixed	Carbon	Film			
Linear	rixed	Metallic	Film			
Lillear		Metallic	Wire wound			
	Variable	(potentiometers	Film			
	Variable	o rheostats)	Wire wound			
Non linear	NTC, PTC, VDR,	LDR, gauges				

Composition resistors

They've been very popular due to their low cost and robustness but now they have become obsolete. They don't have an inductive behavior and a low variation with temperature. They have high mechanic and electric robustness. These resistors are available for low power ranges (up to 4 w).

On the other hand, they present high noise and a decreasing value as frequency and voltage rise. They have poor stability and low precision (tolerance $\geq 5\%$)

Their parasitic capacitance is high thus tending to diminish their impedance.

Carbon film resistors

Pros: low noise, resistance value oblivious to voltage and frequency changes.

Cons: fragility; difficulties to withstand overloads.

They are used for low power applications (up to 6 W). Temperature coefficient is negative, so they can be used to compensate temperature variations.

Metallic film resistors

Several layers of metallic material are laid on an insulator substrate by means of chemical reduction or vaporization.

Their main feature is their stability. They also stand out because of their low noise and the high precision they can achieve.

Wire wound resistors

Metallic wires (metals or alloys) are wound on an insulating cylindrical core (if they were ferromagnetic, we would get inductors instead). The Ni-Cr alloy is used because of its high resistivity and low temperature coefficient. They are coated with an insulating material.

Design parameter are: core diameter (D), wire diameter (d), turn pitch (p), number of turns (n), material's resistivity (ρ). Wire's diameter is determined by the power to be dissipated so the rest of parameters are used to adjust the resistive value:

$$R = \rho \frac{nl_e}{\pi d^2/4}$$
 where $l_e = \sqrt{\pi^2 D^2 + p^2}$ length of each turn

They are used mainly for two types of applications: power and precision.

Power:

There are three types of resistors according to the insulating material used: paint, cement or glass sealed.

Painted resistors	Glass sealed resistors	Cement coated resistors

Nominal power ranges from a few watts to kilowatts.

Precision:

They are used when precision over 1% is required along with stability, low noise levels and power. The inductive effect can be avoided wounding the wire in opposite directions. They are also different types associated with different internal and external insulating materials. The parasitic inductance generates resonant peaks on impedance values.

Linear variable resistors

They include a case, a resistive element and a wiper or spindle. They are called potentiometers or rheostats. These two names are commonly used indistinctively, although in strict sense, rheostats are those connected in series with the load and with the wiper wired to one of the end terminals; potentiometers are then connected in parallel being the wiper connected to the load, as a voltage divider.

TYPES OF VARIABLE RESISTORS

Film: carbon or metallic.

Wire - wound: low power, power and precision.

Carbon film: they are made from a paste of black smoke, liquid bakelite and a plastic laminate. It is laid on a bakelite substrate by rollers.

Metallic film: made up from a mixture of tin and antimony oxide laid on a glass substrate.

Low power wire - wound: their construction and materials used are very similar to those of their fixed counterparts.

Power wire - wound: the Ni-Cr alloy is also used but on a substrate of refractory material to withstand heat.

Precision wire - wound: they use low resistivity alloys (Au-Ag) to obtain low values without increments on diameter. Helical multiturn resistors are among them.

Non-linear resistors

Their resistance varies as a function of physical parameters such as: temperature, light, voltage, etc.

Let's see the most common:

Thermistors: their value is a function of temperature. Their description brings up some new parameters:

Nominal resistance: in this case, the nominal value is given at a certain temperature (25°, typically).

Self-heating: it is phenomenon produced by the increase on temperature generated by the electric current traversing the resistor. As a consequence, the environment's temperature

is misinterpreted. It is quantified in relation with the thermal dissipation factor, which is defined as the power needed to raise component's temperature one degree.

There are two types: PTC (positive temperature coefficient) and NTC (negative temperature coefficient). These coefficients are referred to the sign of parameter α and determine the sign of variation of resistance caused by temperature increments.

Varistors (VDR): their resistance is a function of applied voltage. As a matter of fact, it lowers sharply when voltage rises over a threshold value. They are made up from silicon carbide or zinc oxide.

They are used as protective devices rather than to measure voltage.

Photoresistors (LDR): their resistance depends on incident light. It decreases with increasing light. Once again, they are not usually employed as sensors due to their imprecise variation law. They are rather used for threshold detection.

Capacitors

They are integrated by two conductive plates separated by a dielectric.

They are used to temporarily store energy. The amount of energy they can store depends on their geometric characteristics and the dielectric material used. The capacity of a parallel plate capacitor is:

 $C = \varepsilon \frac{S}{d}$ where S is the area of the plates, d is the distance between them and ε is the permittivity of the dielectric.

For a spherical capacitor: $C = 4\pi\varepsilon \frac{R1}{1 - \frac{R1}{R2}}$ with R2 > R1

Technical specifications:

Nominal capacity: capacity value given by the manufacturer. It is a normalized value. The basic unit is picofarad (at 25°C and 1kHz or 100Hz for electrolytic capacitors)

Tolerance: maximum difference between nominal and real value. It is given as a percentage and is also a normalized value.

Leakage current: electric resistance between plates. It should be infinite but it is actually just very high. It is usually given in terms of μ amps / (volts x μ farad). A maximum or a minimum value is usually given.

Frequency response: It can also be found as *Equivalent Series Resistance* (ESR) or even as a loss factor tan (δ), where δ is the difference between the theoretical phase shift between current and voltage (90°) and the real one caused by the presence of the ESR.

Dielectric strength: the maximum electric field the capacitor can withstand without loss of its insulating properties. Higher field strength turns the dielectric into conductor. It is usually given as a breakdown voltage.

Nominal voltage: maximum voltage that can be applied to the capacitor in a continuous form either in form of DC, peak of AC or the sum of the peak of the AC and the DC component.

Temperature and frequency coefficients: variation of capacity as a function of these two factors due to their influence on permittivity. They are both very complex phenomena so the response is usually provided as a graph by the manufacturer.

Voltage gradient: the maximum rate of increment on the applied voltage. It is closely related to the *maximum instantaneous current* since:

$$i = C \frac{dV}{dt}$$

Maximum ripple current: maximum rms current flowing through the capacitor. It is a function of temperature and frequency.

Classification:

	Without polarity	Ceramic Plastic			
Fixed	without polarity	Others			
	With polority	Aluminum			
	With polarity	Tantalum			
Variable	(trimmer)				

Ceramic capacitors

They are made up from metallic oxides and silicates and are especially adequate for high frequency applications. There are two types:

Class 1: they have high stability and low losses. Their temperature coefficient is linear, known, and constant. The voltage coefficient is close to zero. They are used to build oscillators, filter, etc. These applications need capacitors whose value is known and stable.

Class 2: their value is unstable due to uncertain temperature and voltage coefficients. They also have higher losses. They are use when the exact value of capacity is not relevant such as in coupling and decoupling applications.

Plastic capacitors

They use as a dielectric, various plastic materials such as: polyester (Mylar), polycarbonate, polystyrene, Teflon, polypropylene. According to the dielectric material used, they have different properties that make them suitable for different applications:

Polyester	High capacity. Low voltage, low frequency, general purpose capacitor.						
Polycarbonate	Oblivious to temperature changes. Low voltage, low frequency, general						
rorycarbonate	purpose capacitor.						
Polystyrene	High frequency and voltage applications.						
Teflon	Similar to the previous one but for higher temperature.						
Polypropylene	Similar to the two previous ones but more stable.						

Mica: this is the dielectric material (silicate of aluminum and potassium). They have low losses, broad frequency range and high stability versus temperature and time.

Other materials

There are other materials used in capacitor manufacturing such as paper or glass. They are used for specific applications such as power and high frequency respectively.

Electrolytic capacitors

Although it is not correct to identify electrolytic as polarized, actually in most cases both concepts coincide. So they are sensitive to electric polarity and a reverse voltage may cause their destruction.

Polarity is a setback but the point of electrolytic capacitors is their higher capacity /size ratio. Actually they use micro farads as a reference for their value instead of pico farads. Another relevant advantage is the high ripple current they withstand. Other flaws are: tolerance, losses, and a high and non .linear temperature coefficient.

They are integrated by two electrodes, an electrolyte and a dielectric. The electrolyte provides oxygen to one of the electrodes at fabrication time. The electrode, due to the electrical current applied, oxidizes becoming the oxide formed, the capacitor's dielectric. The electrodes will have to keep the polarity they received at fabrication time throughout their lifetime. Depending on the electrolyte's state, these capacitors are called dry or wet.

There are two main categories:

Aluminum: this is the electrode's material and therefore the dielectric is aluminum oxide.

Tantalum: this is the material used for the electrodes and tantalum oxide is the dielectric formed. It is better insulator than aluminum oxide so these capacitors have a better capacity /size ratio. On the other hand, they withstand lower voltages and are more expensive.

Variable capacitors

The variation of a constructive parameter alters the device's capacity. It is usually the distance between plates of their effective surfaces what is modified. Among them we can find the trimmers, a type of adjustable capacitors whose capacity is modified turning a bolt.

Capacitor type	Capacity range	Nominal voltage range				
Mica	2 pF to 22 nF	250 to 4000				
Paper	1 nF to 10uF	250 to 1000				
Belusturene	10 pF to 4'7 nF	25 to 63				
Polystyrene	4'7pF to 22 nF	160 to 630				
Polyester	4'7 nF to 1'5uF	100 to 160				
	1 nF to 470 nF	400 to 1000				
	47 nF to 10 uF	63 to 100				
Metallic polyester	10 nF to 2'2 uF	250 to 400				
	10 nF to 470 nF	630 to 1000				
	47 nF to 10 uF	63 to 100				
Metallic polycarbonate	10 nF to 2'2 uF	250 to 400				
	10 nF to 470 nF	630 to 1000				
Ceramic Class 1	0'56 pF to 560 pF	63 to 100				
Cerannic Class I	0'47 pF to 330 pF	250 to 500				
	4'7 nF to 470 nF	15 to 50				
Ceramic Class 2	220 pF to 22 nF	63 to 100				
Cerannic Class 2	100 pF to 10 nF	250 to 500				
	470 pF to 10 nF	1000				
	100 uF to 10.000 uF	4 to 10				
Aluminum alastrolytia	2'2 uF to 4700 uF	16 to 40				
Aluminum electrolytic	0'47 uF to 2200 uF	63 to 160				
	2'2 uF to 220 uF	200 to 450				
Tantalum alastrolytic	2'2 uF to 100 uF	3 to 10				
Tantalum electrolytic	220 nF to 22 uF	16 to 40				

Capacity.	value range	and voltaie	of apacitors.
cupacity,	rande range	und ronaje	or upuencors.

Ceramic class 1	Y	The unit is used as a decimal point too.
Ceramic class 2	472	Capacity expressed in numbers equivalent to color code.
Electrolytic	NV 1004F 63V	Capacity in numbers and unit. There is usually a polarity ring and a symbol.
Tantalum		Capacity in numbers and unit. There is usually a "+" symbol indicating polarity.
Metallic polyester	Н 10,415 Ю 1000-	Capacity can be expressed as a number, with color code, etc.
Polyestyrene		

Color code for capacitors.

	А	В	С	D		Е
Calanhand	1 dia:4	2 diait	Multiplier	Toler	ance	Temperature
Color band	1 digit	2 digit		C<10 pF ±pF	C>10 pF ±%	Coefficient ppm/°C
Black	0	0	10^{0}	2	20	0
Brown	1	1	10^{1}	0,1	1	-33
Red	2	2	10^{2}	-	2	-75
Orange	3	3	10^{3}	-	3	-150
Yellow	4	4	10^{4}	-	-	-220
Green	5	5	10^{5}	0,5	5	-330
Blue	6	6	-	-	-	-470
Violet	7	7	10-3	-	-	-750
Grey	8	8	10-2	0,25	-	-
White	9	9	10-1	1	10	-
Gold	-	-	-	-	-	100
Dark blue	-	-	-	-	-	1.500

Tolerance values for capacitors.

Letter	$C < 10 \text{ pF} \pm \text{pF}$	$C \ge 10 \text{ pF} \pm \%$
В	0,1	
С	0,25	
D	0,5	0,5
F	1	1
G	2	2
Н		2,5
J		5
K		10
М		20

Р	0 - +100
R	-20 - +30
S	-20 - +50
Z	-20 - +80

Letter	ppm/°C
А	100
С	0
Н	-33
L	-75
Р	-150
R	-220
S	-330
Т	-470
U	-750
W	-1500

Symbols for temperature coefficients.

Nominal voltage values.

	F	G	Н
	Polyester	Polyestyrene	Tantalum
Black		630	10
Red	250	160	4
Orange			40
Yellow	400	63	6,3
Green			18
Blue	630	25	
Grey			25
White			2,5

Inductors

These components are integrated by a wire wound around a ferromagnetic core.

Like capacitors, the can also temporarily store energy. The amount of energy they can store depends on their geometric characteristics and the core's material.

The inductance of a cylindrical coil is:

 $L = \mu \frac{n^2 S}{l}$ where μ is the core's magnetic permeability, n is the number of turns, S is the core's cross section and l its length.

Their presence in the market is reduced. Where the same result can be obtained by a combination of other components, inductors are avoided due to a number of reasons: electromagnetic compatibility issues, size and weight are the main ones.

Technical characteristics:

Nominal inductance: the component's theoretical value. It is measured in henries.

Tolerance

Loss factor / Q-factor: represent the effect of the equivalent series resistance introduced by the wire. They are determined by tan δ and tan ϕ respectively; where ϕ is the phase shift between voltage and current and δ is 90 – ϕ . In other words:

$$\tan \varphi = Q = \frac{\omega L}{R} \quad \tan \delta = \frac{R}{\omega L}$$

Clasification:

		Filtering chokes with a FeSi core
	Low fraguancy	Air cored for filters
		Power inductors
Coils		Ferrite cored for resonators
		Ferrite cored for RF
	High frequency	Using RF wire (air or ferrite cored)
		Flat (printed on PCB)

PRACTICAL EXERCISE

- > Classify the resistors according to the criteria studied in this activity.
- Check their values and tolerances.
- Classify and measure the capacitors.
- Measure the resistance and check the tolerance of three resistor combined in series and parallel.
- ➢ Find out the value of a coil.
- > Check the influence of light on the LDR's resistance.

INSTRUCTIONS FOR THE ELABORACIÓN OF THE ACTIVITY REPORT:

The report must include:

- > Description of all resistors with their values and tolerances.
- > Description of all capacitors with their values and tolerances.
- > Determine how tolerance behaves when the resistors are combined.
- Calculation of coil's value.
- LDR's values with high and low light.

ACTIVITY 2

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB ACTIVE ELECTRONIC COMPONENTS

OBJETIVES

- Study the different types of active electronic components.
- ➤ Classify them.
- Identify the components in the lab.

EXERCISES

- 1. Components identification.
- 2. TTL & CMOS logic levels.

INTRODUCTION

Back to the classification of electronic components initiated in the previous exercise we will move on to the active ones. Even though it is not easy to give a definition good enough to be valid for the broad variety of active components, we can consider them as those capable of transmitting energy. This meaning that a substantial part of the energy they receive is returned to the circuit although possibly in a different form.

Modern active components are made up from semiconductor materials. It hasn't always been like this, though. In fact, valves dominated the market during a long and important period of time in electronics history.

CLASIFICACIÓN

The classification proposed here is, once again, arbitrary. There are several criteria that can be used to classify components, ours is just one of them.

		Diodes	Rectifier Schottky LED Laser diodes
	Discrete	Bipolar Transistors	PNP NPN Low power Power Low frequency High frequency
ctors	Discrete	Unipolar Transistors	JFET P, N MOS N MOS P
Semiconductors		Controllable power semiconductors	Thyristor SCR GTO IGBT MCT
Se	Integrated	Analog	O.A. Amplifiers Voltage regulators
		Digital	MSI Logic Subsystems Memories Microprocessors, etc.
		Mixed signal	AD converters DA converters

DISCRETE SEMICONDUCTORS

As such we will consider those semiconductors that are encapsulated individually or with a small amount of other devices. We are referring to:

- Diodes: rectifiers, zener, LED, varicap, tunnel, PIN
- Bipolar transistors: npn, pnp, Darlington

- Unijunction transistors: JFET, MOSFET.
- Others: thyristors, triac, IGBT, diac, UJT, optocouplers

There are different regulations affecting the way semiconductors and devices are designated. On the other hand, there are a number of components (especially power devices) that use vendor codes; these won't be considered in our study.

PROELECTRON (European)

There are two types of codes:

Two letters + alphanumeric sequence (consumer electronics). Three letters + alphanumeric sequence (professional uses).

The first letter refers to the semiconductor material:

A: 0'6 to 1 eV gap (Ge).

B: 1 to 1'3 eV gap (Si).

C: 1'3 eV gap (GaAs).

D: less than 0'6 eV gap (InSb).

E: other material such as those used in photo sensors.

The second letter refers to their main typical application field:

A: detection or switching diode (small signal).

B: Varicap diode.

C: Small signal transistor.

D: High power, low frequency power transistor.

E: Tunnel diode.

F: Low power high frequency transistor.

G: hybrid device.

- H: Hall effect sensor.
- L: High frequency high power transistor.

M: Ring modulator-type frequency mixer.

N: Optocoupler.

P: Radiation sensitive device (photodiode).

Q: Radiation generator (LED).

R: Low power control or switching device (thyristor).

S: Low power switching transistor.

T: High power control or switching device.

U: High power switching transistor.

Y: High power rectifying diode.

Z: Zener.

The third letter, if any, determines the type of component. It will be either, X, Y or Z.

Alphanumeric sequence: identifies the model.

There are certain components presenting an additional alphanumeric code as a suffix. It

provides some additional information:

a) Zener diode: One letter followed by the breakdown voltage. The letter "V" is used as the point for non-integer values. It is common to find also the letter "R" indicating that this is a reverse voltage. Before this code a letter indicates the tolerance over the breakdown voltage that follows:

A: 1% B: 2% C: 5% D: 10% E: 15%

b) Rectifying diode: a number and, when it is adequate, the letter "R" (reverse voltage). The number usually corresponds to the maximum repetitive peak voltage.

For small signal professional diodes a color code can also be used. The initial letter sequence is represented by the body color of the device. The alphanumeric code is represented by colored bands. The band closest to the cathode is wider than the rest. The colors are interpreted as follows:

Initial sequence and body colors:

BAV: GREEN BAW: BLUE BAX: BLACK

Numbers and band colors:

0 : BLACK 1 : BROWN 2 : RED 3 : ORANGE 4 : YELLOW 5 : GREEN 6 : BLUE 7 : VIOLET 8 : GREY 9 : WHITE

Examples:

BC107B B: Silicon C: Small signal transistor. 107 B: Model. AAZ15 A: Germanium A: Switching diode Z: Professional use 15: Model

BZY96C3V9R B: Silicon Z: Zener diode Y: Professional use 96: Model C: Tolerance 5% 3V9: Breakdown voltage 3.9 V. R: Reverse voltage

JEDEC This is the American standard EIA RS-236-B, June 1963. The code's structure is:

One digit + N + Alphanumeric sequence

The first digit indicates the number of junctions (1 for diodes, 2 for transistors,...). The letter N refers to silicon as manufacturing material.

To codify diodes a color code can also be used. In this case both the first digit and the letter N are redundant so no visual information is given for them. The alphanumeric sequence is represented by a series of colored bands according to the following rules:

Two digits sequence: one black band followed by two additional band for the two digits according to the table. If a letter comes afterwards another band will be found as explained in the rightmost column of the table.

Number	Color	Letter
0	BLACK	-
1	BROWN	А
2	RED	В
3	ORANGE	С
4	YELLOW	D
5	GREEN	E
6	BLUE	F
7	VIOLET	G
8	GREY	Н



Three digits sequence: three bands representing one digit each. Again, a suffix letter can be represented by a fourth band.

Four digits sequence: four bands representing one digit each. Again, a suffix letter can be represented by a fifth band.

The cathode is usually identified by means of a double width band next to it, normally it is the first digit's band. In other cases all band are equally wide but the huddle on the cathode's side.

Example: 2N5965 2: Two junctions: transistor. N: Silicon 5965: Model.

Packages

In this case we will consider the standard JEDEC as the default option. It uses an alphanumeric sequence to identify packages for both discrete and integrated components. The code is integrated by several fields:

[Features] – [material][position](package) – [form][count]

Among these fields only the package one is mandatory. Nevertheless, if the material is given, the position field must be filled too.

The package field uses two letters, so there are multiple options. Not all of them make sense and, among those that are actually used, we will study those used for discrete components:

CY: cylinder package	
CP: clamped package	
DB: disc-button package	\times
FM: flange-mount package	1000 1000 1000
LF: long-form package	
PF: press-fit package	
PM: post-mount package	

This is not the coding we will find in catalogs since it refers only to types of packages,

not models. In this exercise we will be able to find certain models of packages and to match them with the corresponding JEDEC type.

INTEGRATED SEMICONDUCTORS

They include a number of discrete devices embedded within a single die. They are meant to perform a certain task working together.

There are three types: analog, digital and mixed signal.

Analog components are those who receive an analog signal at the input and produce an analog signal at the output.

Digital components are those who receive a digital signal at the input and produce a digital signal at the output.

Mixed signal components are those who receive a digital signal at the input and produce an analog signal at the output or vice versa.

Some discrete semiconductors, especially the power ones use vendor codes. Concerning integrated circuits, this is much more common, notwithstanding, there are some standards we can study:

PROELECTRÓN

Three letters followed by three digits. First letter: T (analog), F ó S (digital), U (mixed signal) Second letter: makes reference to a feature common to a group of devices: D for MOS family or J for TTL. Third letter: function: A (linear amplifier), H (combinational logic)... First two digits: model. Third digit: operating temperature.

TEXAS INSTRUMENTS

Vendor's ID (SN: Texas Instruments) Two digits for the operating temperature: 74 (0-75); 54 (-55 a 125) Logic family Optional letter N° of bits (optional) Optional field for component's options Function or model Optional field for revision number Package Package additional information

Package

We will take them from the JEDEC standard. For integrated circuits there are several types:

- CC: chip carrier.
- CY: cylinder package.
- FM: flange-mount package.
- FP: flat package.
- GA: grid array.
- IP: in line or in parallel.
- SO: small outline.

NON-ELECTRONIC COMPONENTS

According to their functionality:

Printed circuit boards	Support
Cables	Signal and power delivery
Fiber optic	Optic signal delivery
Connectors	Electric or optical connection
Sockets	Host integrated circuits

Printed circuit boards

According to how components are placed on the board:

Printed circuit board	Through hole components (Class A)	1 side (Type 1)
	Surface mounting devices	1 side (Type 1)
	(Class B)	Both sides (Type 2)
	Both through hole and SMD	1 side (Type 1)
	(Class C)	Both sides (Type 2)

Cables

Copper wires	Coaxial Twisted pair Power wires
Fiber optics	Monomode
	Multimode

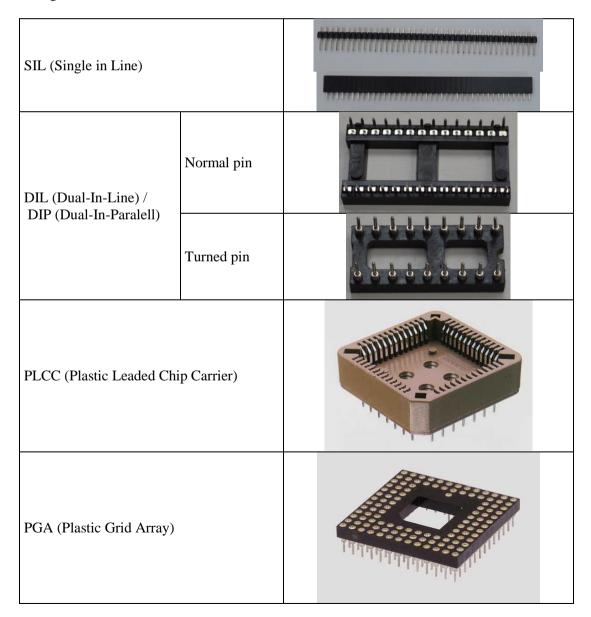
Connectors

For power supply (Not strictly connected with PCB technology))	International: Standard supply connections		
	Industrial		
	DC. Jack		
	Rectangular general purpose		
	Terminal strips		
	Custom made		
Signal	Sub D, DB9, DB25		
	IE 488		
	SCSI, SCSI 2		

	USB	
	Other standards: FCC-68, DIN 41612	
	Single wire	
For ribbon cable		
For memory devices and cards		
For PCB connection	Pin strips	
	Screw PCB terminals	
	Insertion PCB terminals (male or famale)	
For coaxial	BNC	

Sockets

Through hole sockets:



Are used for 30 and 72 way memory modules They include plastic or metal locks, are low insertion force and are right wise polarized. Pin pitch, 30 way - 2,54mm. 72 way - 1,27mm

PRACTICAL EXERCISE

- Identification of components.
- ➤ Use NOT gates to check TTL & CMOS logic levels.
- Identify types of IC packages.

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT:

The report must include:

- > Description of components and packages.
- Logic levels measured.

ACTIVITY 3

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PRINTED CIRCUIT BOARD DESIGN

OBJETIVES

- > Introduction of concepts related to printed circuit board design and technology.
- > Familiarize with the different possibilities and techniques available.
- Carry out manual design.

EXERCISES

1. Design of a PCB for the circuit proposed.

INTRODUCTION

We will start from a schematic and will try to come up with a PCB layout for it.

The schematic may be a paper sheet or a computer file. It may have been simulated so we can have a certain guarantee of its prospective performance. If no simulation has been conducted it is very advisable to go through a prototyping phase before.

There are different prototyping processes:

- Using prototyping board where components are connected through cables and embedded electrical connections. No soldering is involved.
- Wire wrapping. Components are inserted in a drilled board and connected with special wires wrapped around the terminals.
- Strip board: These boards have strips of holes electrically connected. Traces are cut where adequate once the components have been soldered. When electrical connections need to be extended to other rows, additional wires have to be soldered.
- Prototyping board: it is also a predrilled board. Unlike the previous one, components are clamped not soldered. Holes are internally connected following certain patters. Other connections can be made with external wires that are also clamped.

We will assume that, before manufacturing the PCB, we are quite sure that the circuit has been correctly designed.

Printed circuit boards interconnect components through copper tracks.

TRADITIONAL PROCESS	COMPUTER ASSISTED AND AUTOMATED PROCESS
Schematic	Schematic capture: schematic editor with libraries of symbols and packages. Analog, digital, thermal and mechanical simulation. Component list, prices, etc.
Component placement and board routing	PCB (Print Circuit Board): component placement Auto-routing Drilling layout.

List of processes to be followed in the elaboration of a PCB, according to their degree of automation:

	Solder mask.	
Design transfer (draw with a permanent marker or use or stickers)	Routing mask	
	Printer, plotter, photoplotter, etc.	
Chemical etching of the exposed parts of the copper coating.	CNC track milling.	
Manual drilling	Automated drilling	
Insertion of components	Automated component insertion	
Manual soldering	Wave or other automated soldering	
Mechanization		
External wiring (power and signal)		
Test		

TYPES OF DESIGN PROCESSES: MANUAL, COMPUTER ASSISTED.

The differences between the design processes have to do with the degree of automation.

Manual design

It is not automated whatsoever. The quality of the result very much depends of the technician's expertise.

Computer assisted

A computer will be necessary in all cases. There are different degrees of automation though.

Computer assisted manual design

The computer is basically a tool to get a better looking result. It is used mostly as a drawing tool.

Semi-automatic

The computer conducts part of the job. The technician places components on the board, establishes connections and draws the tracks. Sometimes the process is considered semi-automatic even if the computer routes the board.

Automatic design

The computer places components and routes de board completely. No decisions are made by the technician. Nevertheless, routing strategies, design rules and necessary conditions to accomplish can be set beforehand.

MANUAL DESIGN

A computerized schematic or a paper design makes no difference when making a manual design.

We will need to know the exact measures of all components to be placed including mechanical devices such as heat sinks.

We will usually work in a scale higher to real size, i.e. 2:1.

Place components in a way that the highest possible number of connections can be directly drawn. Draw as many connections as possible avoiding track crossings since they would become short-circuits in the final board.

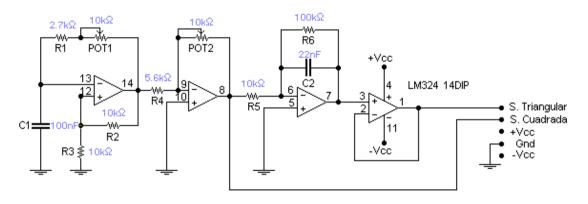
If the routing is not finished, rearrange components so more connections can be sorted. Even if the design is complete, it is recommendable to try different options in order to minimize board size and track length.

Down scale the design to its real size (1:1). Pay attention to some design hints first:

- Track width is irrelevant when the current is very low. Nevertheless when the board is to be handcrafted it is advisable not to work under 0,5 mm. If the current is expected high, the track width has to be increased accordingly. For a 2 A current, and a 35 µm copper thickness, track width must be 0,7 mm. For 5A at least 2 mm are required.
- Power and ground tracks are usually wider than the rest.
- The distance between tracks depends on the voltage. It should be at least 0,4 mm for voltages up to 100 V. Every 100 V the distance should be increased 1mm.
- The copper area around each terminal where the soldering process will take place usually doubles the terminal's diameter. A 3 mm pad makes the manual soldering easy but it is not always possible since it may overlap neighboring pads. It is also advisable to avoid ample copper areas especially in the proximity of component terminals since they tend to spread the heat when the terminal is being soldered.
- Right angles should be avoided; 135° turns are recommended.
- Do not forget to create the drills necessary to assemble the PCB to its casing.
- The PCB will look better if the parts are correctly and symmetrically aligned.
- Try to avoid routing tracks between IC terminals since they make the etching process more challenging. Between the two terminal rows of an IC, no more than three parallel tracks are recommended for the same reason.
- Connectors must be places close to the board's edge.

PRACTICAL DESIGN

Design a PCB for the following schematic:



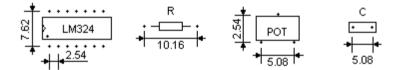
Carry out:

- PCB silk screen mask: including the final position of all parts.
- PCB track layout.

PRECONDITIONS:

No more than 3 tracks can be place in parallel under an IC's body. No tracks can be routed between the terminals of an IC. No more than 4 tracks under a resistor. No more than one track under a capacitor. No more than one track between the connector and the board's edge. No tracks under the potentiometer.

Footprints to be used. Sizes in mm:



Activity: 3

PRÁCTICAL EXERCISE

- Sketch the design first to solve the routing.
- > Convert it to real size.
- > Trace it on a transparent piece of paper (or scan it and then print it on acetate).

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT

The report must include:

- ➢ Layout sketch.
- Real size design on a transparent paper.
- Description of the steps followed.

Attachment:

To help with the real size work an inch size graph paper is provided.

Industrial Elec	tronics &	Automation	Engineering
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Activity: 3

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ACTIVITY 4

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PRINTED CIRCUIT BOARD DESIGN II

OBJETIVES

- ➢ Use of CAPTURE program to create schematics.
- > Footprint configuration.
- Netlist generation for LAYOUT.

EXERCISES

> Introduction of the proposed circuit in Orcad software package.

Activity: 4

INTRODUCTION

We will assume that the student is already familiar with the use of the Orcad package in general and with the Capture program in particular. Being that the case, the first step of this exercise will be the creation of a schematic for the circuit proposed in the previous exercise. In the next table the libraries where the parts used in this circuit can be found:

Resistors	Capture\library\PSPICE\ANALOG.OLB
Capacitors	Capture\library\PSPICE\ANALOG.OLB
Potenciometers	Capture\library\PSPICE\BREAKOUT.OLB
LM324	Capture\library\PSPICE\OPAMP.OLB
5 way connector	Capture\library\Connector.olb

FILE GENERATION

Let's start from the schematic introduced in CAPTURE.

Footprints

Before generating more files it is necessary to configure the footprints for all parts.

Edit each part's properties and check there is a footprint defined. In many cases the default footprints are right but, in certain ones, the footprint property is empty. There are some cases, though, where the part has a footprint but it is not correct for the PCB program. It is usually a syntax mismatch. In order to sort this out a list of correct footprint for all the parts used in this exercise is provided:

LM324	DIP.100/14/W.300/L.800
R1, R2, R3, R4, R5, R6	AX/.300X.100/.028
C1	RAD/.300X.125/LS.200/.031
C2	RAD/.300X.125/LS.200/.031
POT1, POT2	VRES51
CONECTOR	SIP/TM/L.500/5

Output file '.MNL'

The LAYAOUT program collects all the information it needs from a netlist file whose extension is: '.MNL'.

This file is generated by CAPTURE when the current schematic page is selected (file SCHEMATIC1/PAGE1 by default) and clicking on the 'TOOLS' menu:

CrCAD Capture						
File Design Edit View	Tools	PSpice	Accessories	Options	Window	He
File Design Edit View	B U D C C C C B B E I T r G G S I A	nnotate ack Anno pdate Pro esign Rul reate Net reate Diff ross Refe ill of Mato xport Pro enerate P polt Part ssociate F	tate operties es Check erential Pair erence erials perties perties art	Options	Window	He → → → → → → → → → → → → →
	P	oard Sim	LM	324	ľ.	
			1 1 1 1	3 🔨 🧯		

We will see the following dialog window where we must select the netlist for LAYOUT:

Create Netlist	×
PCB Editor EDIF 2 0 0 INF Layout PSpice SPICE Verilog VHDL Other	
PCB Footprint	
Combined property string:	
{PCB Footprint}	
Ontings	
Options	
Run ECO to Layout	
O User Properties are in inches	
User Properties are in millimeters	
Netlist File:	
G:\MANUAL TESIELEC\MANUAL.MNL Browse	
Aceptar	Ayuda
	.,,

Right after a new output file will show up at the output part of the Project management window (Design Resources/Output).

The ECO options will automatically inform about the changes in the schematic that may affect the PCB design.

Pay attention at the units (mm) used in both schematic and PCB design. They must match to avoid fatal errors in the design.

INSTRUCTIONS FOR THE ELABORATION OF THE ACTIVITY REPORT

The report must include:

- Circuit schematic.
- > Description of the steps taken to get to the design.
- > Comments on the difficulties encountered during the design.

ACTIVITY 5

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PRINTED CIRCUIT BOARD DESIGN I I I

OBJETIVES

- > Introduction to LAYOUT. Common features for all modes.
- > Get to know different ways to work with CAD programs.
- Manual design of PCB using OrCad Layout.

EXERCISES

➤ Use Orcad to obtain a final PCB design for the circuit proposed in previous exercises.

INTRODUCTION

In this activity we will connect CAPTURE's output with the PCB design program.

LAYOUT PROJECT CREATION

Once the schematic has been finished and stored, and the netlist file has been generated, we can start a new LAYOUT project.

We will proceed as follows:

- Start OrCAD-LAYAOUT
- Select FILE/new
- Then the technical template 'METRIC.TCH'.
- Load the netlist file generated by CAPTURE.
- Name the new Project. A '.MAX' file will be instantly created.

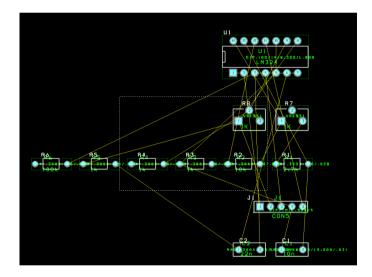
AutoECO	X
File Names	
Input Layout TCH or TPL or MAX file	MRU ÷
C:\orcad\0rCAD_16.0\tools\layout\data\metric.tch	Browse
Input MNL netlist file	
G:\manual tesielec\MANUAL.MNL	Browse
Output Layout MAX file	
G:\manual tesielec\MANUAL-1.max	Browse
□ Overwrite MAX file without warning	
Options	
AutoECO Start a new board file. Choose an appropriate technology or template file as your input TCH file. If updating an existing board, nets and components will be updated. No property changes on existing nets and components (no Footprint cha When a pad's net changes, ripup the entire track rather than just the last s Any special switches given to you by Cadence Customer Support	inges).
Use design library only	Edit Library Browse
AutoECO Apply ECO Help	Cancel

If the footprint configuration process has not been successful, the following window will inform us about the errors:

Link Fo	potprint to Component	X
Auto	©ECO cannot find the footprint TO-92MOD for component	Q5.
	Please choose one of the options below:	
	Link existing footprint to component	
	Create or modify footprint library	
	Defer remaining edits until completion	
	OK Help Cancel	

Any of the three alternatives can be taken but it is more advisable to go back to CAPTURE and fix the configuration.

Once everything is correct, we will see the following screen:



The dotted line represents the area where the design rules are checked. At this stage we recommend removing it by clicking on the DRC button.

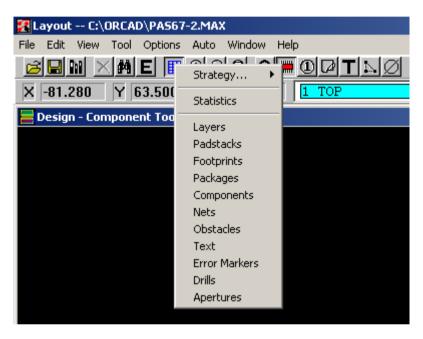
ANUAL-1.MAX	
Auto Window Help	
) q = 0 q t l q : = = : : : : : : : : : : : : : : : :	
3 1.270 1 TOP Online DRC	
N)	

CONFIGURATION PARAMETERS

We have to set the design rules before starting our work with the PCB:

Single sided routing	
Track width	0'8 mm
Track separation	0'8 mm (do not set)
External diameter for DIP and connector	2 mm
Drill	0'5 mm
External diameter for other parts	2'5 mm

These adjustments are made on their spreadsheet which can all be found after clicking the spreadsheet button:



Setting the routing layers

The sheet "layers" shows layer properties concerning its routing capabilities. To set single layer routing, "top" layer has to be configured as "Unused".

_ayers				-
Layer	Layer	Layer	Layer	Mirror
Name	Hotkey	NickName	Туре	Layer
ТОР	1	TOP	Unused	BOTTOM
воттом	2	BOT	Routing	ТОР
GND	3	GND	Plane	(None)

To do so, we double click on the top layer to go to the properties window:

Edit Layer	X	
Layer Name	ТОР	
Layer NickName	ТОР	
Layer LibName	ТОР	
Layer Type		
C Routing Layer	O Plane Layer	
Onused Routing	C Documentation	
O Drill Layer	O Jumper Layer	
Mirror Layer Layer Name BOTTOM		
Jumper Attributes OK Help Cancel		

Selecting 'Unused Routing' option, no track will be routed on this layer.

Setting pad size

The "Padstacks" option grants Access to the padstack spreadsheet where all pads properties can be displayed and modified. However, this spreadsheet is enormous since it includes even parts that are not present in our design. To make configuration easier, it is a good idea to first select a component with the "component tool":

ع ا	Layout G:\MANUAL TESIELEC\MANUAL-1.MAX										
File	Edit	View	Tool	Options	Auto	Window	Help				
Ê	; <mark> </mark>						D et Ng		1 <u>2</u> H	77	🚦 💞 SE
X	X -83.820 Y 60.960 G 1.270 Component Tool										
	Esign - Component Tool (DRC OFF)										

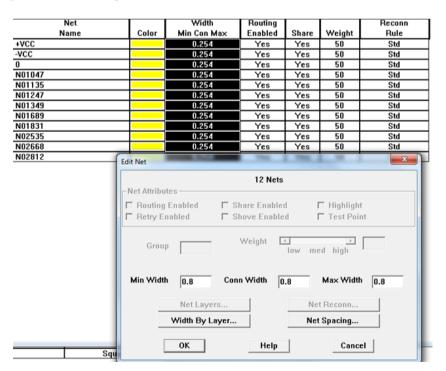
Before moving to the padstack spreadsheet we will press "scape" to unselect the component. It may seem that we've done nothing but we will see that, after selecting the spreadsheet we will have landed on the just unselected component's properties. Notwithstanding, the description of pads within a single part is still complex. The spreadsheet will display a description for all types of pads in the component. Each one will contain its shape and size in all possible layers. Bear in mind that our parts have one or two types of pads. For instance, the IC has a square pad on terminal one and a round one on the rest. Since we are going to work on the bottom side only we will have to care about just two layers:

- "bottom": for the external diameter of the pad.
- "drill": for its internal diameter.

SIP.IIb_pad1					
TOP		Square	1.397	1.397	0.000
BOTTOM		Square	1.397	1.397	0.000
GND	Edit Padstack Layer	Tapane	× F	1.905	0.000
POWER	Eurit Paustack Layer	Taxan .	5	1.905	0.000
INNER1	Padstack "SIP.IIb	_pad1", Layer "BOTTOM"	7	1.397	0.000
INNER2			7	1.397	0.000
INNER3	□ Non-Pla	tod	7	1.397	0.000
INNER4			7	1.397	0.000
INNER5	Use For		7	1.397	0.000
INNER6		hermal Relief	7	1.397	0.000
INNER7	Elood Pl	anes/Pours	7	1.397	0.000
INNER8	-Pad Shape		7	1.397	0.000
INNER9			7	1.397	0.00
INNER10	C Round	C Oblong	7	1.397	0.00
INNER11	C Square	C Rectangle	7	1.397	0.00
INNER12	C Oval	C Thermal Relief	7	1.397	0.00
SMTOP	C Annular	C Undefined	7	1.397	0.00
SMBOT			7	1.397	0.00
SPTOP	E No.	Connection	D	0.000	0.00
SPBOT	L NU	Connection	D	0.000	0.00
SSTOP	Pad Rotatio	in:	D	0.000	0.00
SSBOT		1	D	0.000	0.00
ASYTOP	Pad Width: 2.2	Pad Height:	1	1.397	0.00
	X Offset:	Y Offset:			
	OK	Help Cancel			

Setting the track width

We will go to the "Nets" option in this case.



As it is our circuit, the spreadsheet is very simple. We can set the width individually for each track but, if all of them are to be equally wide we can click ion the heading to select and modify all at once. The three parameters we encounter are set at 0,8 mm.

PLACING THE COMPONENTS

With the component selection tool we can move the parts to any location. As a result of exercise 3, we already have a very precise idea of how to arrange them. We can set place and routing grids if that makes our work easier.

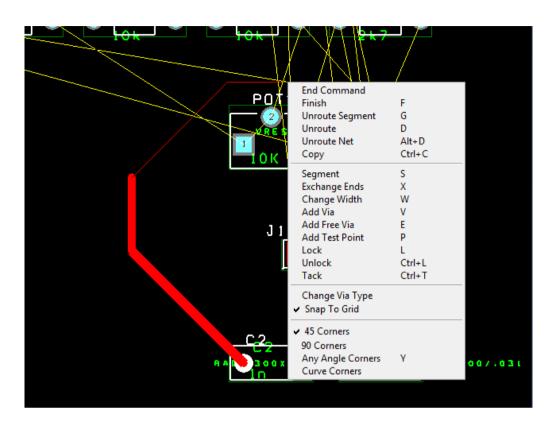
MANUAL ROUTING

If we have decided not to use a place grid, we may find that our components are placed either too close or too distant when we try to route the tracks. Since this is our first attempt it is even positive to make the process a bit interactive and try moving the components and re-routing the tracks.

Although there are several tools to draw track we will use only the one that permits free routing:

MANUAL-1.MAX		1140
Auto Window Help		
PP Q B D P T N	Ø 📲 🎫 🖬 🥑 州	ㅋ 🏞 🚦 👯 🏹
G 0.254	•	Add/Edit Route Mode
e Mode (DRC OFF)		

For the following steps it is important to keep in mind that, in this program the right click is constantly used. All options affecting the different tools are available through this button. The following figure shows the routing of a track and the different options available. The most important are "Finish" (to automatically end the remaining part of the track), and those to unroute totally or partially a track. It is also important to remember that routing is not a dragging operation on the mouse but a single click at each end.



FINISHING THE DESIGN

Once all tracks are drawn, there are a number of steps to follow so we have our design ready for manufacturing.

Board outline

Using the obstacle tool we will surround the design with a board outline. It is usually a rectangular shaped thick line separated from any other element in the design by at least a track width. There's no maximum distance but drawing it too far would make the PCB grow unnecessarily.

NUAL	TESIELEC	MANUA	L-1.MAX	_				-	_	_
Tool	Options	Auto	Window	Help						
<u>å</u> E		ΩD		D 🔽 🕇	Ø⊿		Ħ	<u>5</u> H	∄⊅	🚦 💕 <u>SF</u>
61.	.976	G 0.2	54	Obsta	acle Too	l		-		
cle To	cle Tool (DRC OFF)									

Once the obstacle tool has been selected, the right click will allow the creation of a new obstacle. Another right click will grant access to its properties sheet where we will state that it will be a board outline.

Edit Obstacle		— ×—
Obstack	e Name 123	
Во	Obstacle Type ard outline	×
Group He	ight Width	1.27
	Obstacle Laye	r
	Global Layer	-
	Global Layer	
Copper Pour Rules	TOP BOTTOM	
Clearance	- GND	
	POWER INNER1	
Note: Use Pin	TINNER2	opper Pour Seed'
	INNER3 INNER4	ints
Isolate all tracks	INNER5	■designated object
Net Attachmer	nt (" ^y " for none):	-
🗖 Do Not Fill	Beyond Obstacle E	dge
Hatch Patte	rn	Comp Attachment
ОК	Help	Cancel

We will place it in the bottom layer since this will be the layer from which the design is to be transferred. Drawing this line is not intuitive unfortunately. Once again we have to remember that the usual "dragging" doesn't work as expected in LAYOUT. We may need several attempts to come up with it.

Text tool

This tool will give us the possibility of writing on the design. This writing will be transfer to copper later, so it must be separated from any other element to prevent short-circuits.

SIELEC	MANUA	L-1.MAX					
	-						
Options	Auto	Windo	w Help				
⊞ 🗩	QQ	Q 🖽		Ø	<u>5</u> H	∄⊅	🚦 💞 <u>SF</u>
46	G 0.2	254	2 BOT	ext Tool	•		
C OFF)							

A right click will take us to the options where we can add a new piece of text. In our case the text to be inserted has a double purpose:

- To identify the author of the design.
- To serve as a reference to place the mask on the ultraviolet exposure machine.

In order to fulfill the second purpose, the text has to be inverted ("mirrored"), since it has to be rea don the bottom layer.

Text Edit			×					
	Text 85							
-Type of Text-								
Text	String Ejem	plo						
• Free	, -	C Custom Pr	-					
C Reference C Componen	•	 Package N Footprint N 						
Line Width Rotation	Text lo 0.254	ocation [*,*] Text Height Char Rot	0					
Radius	0.	Char Aspect	100					
	⊡ Mi	rrored						
Layer:								
	Comp	Attachment						
ОК		Help	Cancel					

Size and width can be modified to fit the text into an available gap in the board. If the lines are too thin though, they may vanish during the etching process.

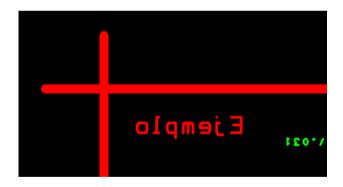
Reference marks

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB

We will use the obstacle tool again for this step. The reference marks are important for our handcrafted manufacturing process since they will prevent any misalignment during the ultraviolet exposure. The type of obstacle to be selected in this case is "free track".

lit Obstacle			
()bstacle Name	125	
	Obsta	cle Type	
	Free trac	ok -	•
Group	Height	Width	1.27
	Ob BOTTO	stacle Layer	-
Copper Pour Rul	es		
Clearance		Z	order
Note: U	se Pin Tool cor	nmand 'Togg	le Copper Pour Seed'
		pper pour see	
☐ Isolate all tra	cks E	Seed only fr	rom designated object
Net Att	achment (""' fo	r none):	-
□ Do M	lot Fill Beyond	Obstacle Edg	ge
Hate	h Pattern		Comp Attachment
OK	_	Help	Cancel

The most common shape for the reference marks is, as depicted in the following picture, a prolongation of the board outline at its corners.



PRINTING

The "file" menu gives us Access to the print options but, before printing, make sure all layers except bottom have been made invisible.

Select options "Keep drill holes open" and "Force Black & White".

Print/Plot	
Print/Plot Format	Print/Plot Settings
Title: MANUAL-1	X Shift: 0
○ DXF	Y Shift: 0
 Print Manager Keep Drill Holes Open 	Center on Page 🗖 Mirror
Print/Plot Current View	Scale Ratio: 1 To: 1
Force Black & White	Rotation(CCW)
🗖 Print/Plot To File	• 0 · · 90 · · 180 · · 270
File Name: manual-1.prn	
,	
ОК Не	lp Cancel

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT

The report must include:

- > PCB design obtained.
- > Description of all steps followed to get to this result.
- > Comments on the main difficulties encountered.

ACTIVITY 6

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB AUTOMATIC PRINTED CIRCUIT BOARD DESIGN

OBJETIVES

- > Carry out a completely automatic PCB design.
- Auto placement of the components will not possible though.
- > Auto routing.
- Configuration of parameters and strategies.

EXERCISES

> Automatic PCB design with LAYOUT.

INTRODUCTION

In previous exercises we've experimented how to connect the schematic capture program with the PCB designer; now we will find out what the PCB program can make automatically. The main tasks to be carried out automatically by one of these programs are: auto place of components and auto route of tracks.

The starting point for this exercise will be the configuration of design rules: "Layers", "Padstacks" and "Nets".

COMPONENT AUTO PLACEMENT

The auto place option is not present in all programs and versions. OrCAD suport this option only in the LAYOUT PLUS version.

Auto place requires a correct definition of all components in the netlist file. This has already been achieved in previous exercises. Since our laboratory version of LAYOUT doesn't include this feature, we will have to place the parts manually. This has also been done in exercise 5 but in this case he might need to separate or move some parts to facilitate the auto routing.

AUTO ROUTING

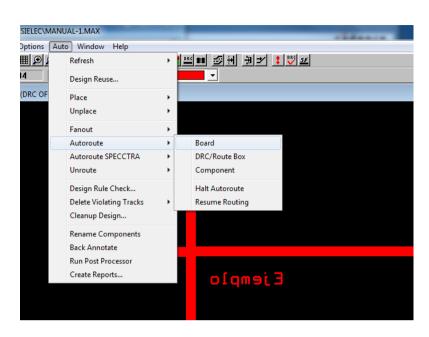
Before ordering the auto routing of the board, we have to set the board outline. We have no previous constraints on the board's size but we should keep it reasonable. If it turns out to be too small for routing, we can widen the outline and try again.

Single sided routing

Using the same settings as in previous exercise, we can proceed to single side routing. To do so we just need a click as seen in the following figure.

With the design rules we have set, it is difficult for the program to come up with a complete design. We may try changing the location of the parts of increasing the board size. It is a very dynamic process since the "Unroute" option deletes all tracks simultaneously.

The routing algorithm can be configured too but it is beyond the scope of this course deepening in routing algorithms.



Double sided routing

Given the difficulties to obtain a single sided auto routing, we will also try a double sided one. To do so we simply need to return the Top layer to its default value: "Routing".

Having done this, just click the auto route option again.

DOCUMENTATION

Files

We can collect some information from our design. The option AUTO/Create Reports we give us the possibility to store several types of data. Let's try them all:

Comp All (Comps)	Drill Pairs (Lev1 Lev2)
Comp Bottom SMT (Smbot)	Net Lengths (Netlen)
Comp Bottom Thru (Thbot)	Net List (Netlist)
Comp Insertion (Insert)	Padstacks (Padstack)
Comp Top SMT (Smtop)	F Part List (Partlist)
Comp Top Thru (Thtop)	F Pins Unused (Unusepin
Connections (Conn)	🗆 Renames (Rename)
Conns Unrouted(Unroute)	Statistics (Stats)
Cross References (Xref)	Test Points (Tpoint)
Drills (Drill)	🗆 Vias (Vias)
Append to Existing Rpts	View Report(s)
Use Default File Names	Save As File(s)
Use Current Design Directory	· · ·
Browse	Save Settings
Select Cus	tom Reports
Net Properties Report (Netp Component Properties Repo Pick and Place Report (Pick	rop) rt (Compprop)

The most useful options may be:

- [Component List (Generic)], Where we can find all types of elements in our design and the number of elements of each type.
- The statistics option permits comparisons between different designs. They can also be printed on the screen selecting View/Database/Statistics
- Unusepin, highlights unconnected terminals so we can detect design mistakes.

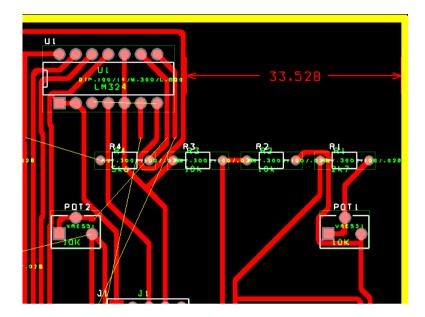
Graphics

Another interesting tool is the density graph that can be retrieved from VIEW/Density Graph

Dimensions

We can generate a Data Exchange Format (DXF) file which in this case is a graphics file that includes board dimensions. It can be accessed through **Tool/Dimension Tool**.

It is also possible to measure distances between different spots within the design through **Tool/Measurement tool.**



Orcad provides also a Visual CAD tool accessible through the TOOLS menu. It is a complete graphic design program.

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT

The report must include:

- Double sided design.
- ➢ Single sided design.
- Comparison between the two, using the statistics generated by the program. Remark pros and cons of each type of design.

ACTIVITY 7

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PCB POST PROCESSOR

OBJETIVES

- ➢ Finalize project documentation.
- > Post process design for manufacturing.

EXERCISES

➢ Generation of Gerber files.

INTRODUCTION

When it comes to industrial manufacturing of PCB the manufacturer some additional documentation must be generated and provided to the manufacturer. To do so we will have to post process the design. Since the manufacturers are not affected by the restrictions we have in the lab, we will work with the double sided design.

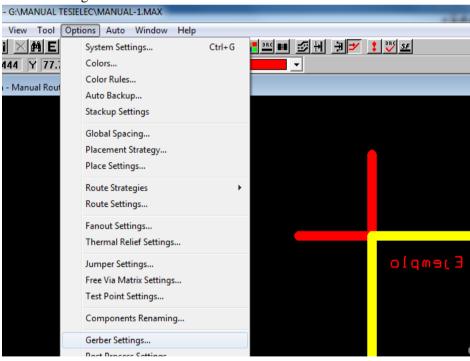
PCB POST PROCESSOR

We are expected to generate and deliver a comprehensive set of documents. EDA software packages such as Cadence are designed to generate it automatically. There are many format available but, what most manufacturers require is the following:

- A Gerber file, usually RS-274X (Extended Gerber) formatted where the different layers integrating the board are described. It will contain all steps to be followed to accurately draw tracks, pads, serigraphy, etc.
- o An Excellon formatted file describing drill positions and diameters.

A number of steps must be followed to comply with those requirements:

1. Adjust documentation file generation settings. This can be done through: Options > Gerber Settings.

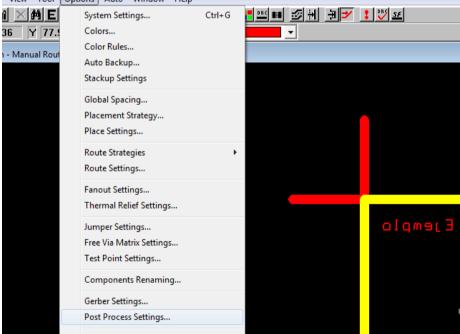


2. Default settings are valid for most manufacturers.

Plot output	Batch			
File Name	Enabled	Device	Shift	Plo
*.TOP	Yes	EXTENDED GERBER	No shift	Top Layer
*.B0T	Yes	EXTENDED GERBER	No shift	Bottom Layer
*.GND	Yes	EXTENDED GERBER	No shift	Ground Plane
*.PWR	Yes	EXTENDED GERBER	No shift	Power Plane
*.IN1	No	EXTENDED GERBER	No shift	Inner Layer 1
*.IN2	No	EXTENDED GERBER	No shift	Inner Layer 2
*.IN3	No	EXTENDED GERBER	No shift	Inner Layer 3
*.IN4	No	EXTENDED GERBER	No shift	Inner Layer 4
*.IN5	No	EXTENDED GERBER	No shift	Inner Layer 5
*.IN6	No	EXTENDED GERBER	No shift	Inner Layer 6
*.IN7	No	EXTENDED GERBER	No shift	Inner Layer 7
*.IN8	No	EXTENDED GERBER	No shift	Inner Layer 8
*.IN9	No	EXTENDED GERBER	No shift	Inner Layer 9
*.110	No	EXTENDED GERBER	No shift	Inner Layer 1
*.111	No	EXTENDED GERBER	No shift	Inner Layer 1
*.112	No	EXTENDED GERBER	No shift	Inner Layer 1
*.SMT	Yes	EXTENDED GERBER	No shift	Soldermask T
*.SMB	Yes	EXTENDED GERBER	No shift	Soldermask E
*.SPT	No	EXTENDED GERBER	No shift	Solder Paste
*.SPB	No	EXTENDED GERBER	No shift	Solder Paste
*.SST	Yes	EXTENDED GERBER	No shift	Silkscreen To
*.SSB	No	EXTENDED GERBER	No shift	Silkscreen Bo
*.AST	Yes	EXTENDED GERBER	No shift	Assembly To
*.ASB	No	EXTENDED GERBER	No shift	Assembly Bo
*.DRD	Yes	EXTENDED GERBER	No shift	Drill Drawing

3. Now adjust post process settings.

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View	Tool	Ontions	Auto	Window	Help	



- 4. Again, default settings are OK.
- 5. Finally though Auto > Run Post Processor, the documentation will be generated.

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Back Annotate Collome		Delete Violating Tracks	•
			E jemplo
Create Reports			
		Create Reports	

DOCUMENTATION DELIVERY

As a result of the previous process, a number of files have been created. They will be sent to the manufacturer:

- A *.lis. file will be created and opened automatically when the postprocessor ends. It includes a summary of all apertures in the different layers within the board.
- The "thruhole.tap" file where drill information complying with the Excellon format is included.
- A number of files whose extensions coincide with layer's names. They contain the Gerber formatted design of each layer.
- Gerber documentation file *.drd.

All these files are relevant to the manufacturer and must be packaged together before shipping.

INSTRUCTIONS FOR THE ELABORATION OF THE ACTIVITY REPORT

This activity does not require the usual report. Instead, a compressed file containing all the documentation files must be uploaded.

Remark: Before uploading the files, they must be checked for correctness. A Gerber editor can be used for this purpose. There are many free online editors that can be used, such as: http://www.gerber-viewer.com/

ACTIVITY 8

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PRINTED CIRCUIT BOARD MANUFACTURING. PHOTO PROCESS

OBJETIVES

- > Get to know and carry out the photo process for PCB manufacturing.
- ➢ Make the final PCB design.

EXERCISES

- Print the PCB design in paper.
- > Print the PCB design in acetate.

INTRODUCTION

This process replaces the traditional manual process meant to manufacture one single board.

In that manual process, once the PCB has been designed, it is drawn directly on the copper layer with an acid resistant ink.

STEPS ON A TOTALLY MANUAL PROCESS:

- Cut the board to its final size. Use a saw or a guillotine.
- Sand the edges.
- Wash it with a scrubber and soap.
- Rinse it until no cleaner remains.
- Dry it up.
- Draw the track and footprints straight on the copper coating with an indelible marker. There are stickers on the market to make the pads easier to draw.

The rest of the process coincides with the photographic one.

PHOTO PROCESS

As already stated, when a number of exemplars of the same design have to be built, the photo process is recommended.

It involves the following steps:

1. Print the design on a material transparent to ultraviolet light. This result in a photo mask to be used in the following steps.



TIPS: When the printer lacks of a good resolution (dots per inch) the mask may not be dense enough and the light may go through the tracks. It is a good practice to print out two copies and stick them together.

Laser printers have a resolution from 300 ppi, whilst the minimum should be 600 ppi for a good job.

- 2. The board to be use must be big enough for the design. It will be coated with a photoresist layer around 2,5 μ m thick; it will be initially protected by a black sheet of adhesive plastic. The base material may be either fiberglass or phenolic paper.
- 3. Remove the protective plastic and try to avoid long exposure to natural or ambient light since they all have an ultraviolet component.

- 4. The mask has to be attached to the board (resist side) avoiding any gap that may distort the image. They both go to the exposure machine. It is important to take note of the time required for an adequate exposure since each machine has a different one.
- 5. After the exposure, the board is introduced into a developer solution. The part of the resist that has received the light is removed. We assume that the photoresist a positive resist is used. It is recommendable to swing the developer a litter to obtain a homogeneous development.
- 6. When the circuit can be clearly seen, the development is complete. Wash the board with water to stop it and prevent the removal of the resist remaining.
- 7. Introduce the board into the etching solution and swing it a little.
- 8. When the copper has been removed, wash the board again to eliminate the acid and the rests of copper.

Remark: Some boards have a negative resist coating. In this case the development process removes the part of the coating that hasn't received the light. The mask has to be negative too for a proper result.

Our design package includes a GERBER TOOL meant to verify the PCB as well as other post processing and pre-manufacturing jobs. With this tool it is possible to place several copies of the design in a bigger sheet thus optimizing the manufacturing of small and large series.

CHEMICAL ETCHING

The board is submerged into a corrosive bath to eliminate all copper that is not part of the circuit. Take note of the products used and their relative quantities to be able to do the same process in the future.

Safety:

These products can be highly damaging so the use of protective elements is mandatory: rubber gloves, apron, glasses. If the solution reaches the skin or eyes wash the affected area with abundant water and search for medical assistance if necessary.

All containers used in this process must be made from plastic or glass. In case the waste product has to be temporarily stored it has to be kept in a hermetic container. Ferric chloride is a hygroscopic product so it tends to absorb water and might spill over the container otherwise. Currently the products can be found as a combination of a liquid and a solid one. The containers are sold in sizes that match the exact proportions to be used. Being sold separately most dangers are avoided.

As the process is developing, the current state of the board has to be periodically checked to prevent an excessive etching that could damage the circuit.

Once the etching is finished, the board has to be washed again.

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT

The report must include:

- Detailed description of each process.
- Paper designs.
- Photo mask.

ACTIVITY 9

TECHNOLOGY OF ELECTRONIC SYSTEMS LAB PRINTED CIRCUIT BOARD MANUFACTURING (II)

OBJETIVES

- > PCB drilling and component insertion.
- ➢ Manual soldering.
- > Verification.

ACTIVITIES

- ➢ Drilling
- ➢ Insertion
- > Soldering
- > Verification

INTRODUCTION

The PCB has already been manufactured so we just have to solder the components and check the result work fine.

FINAL PROCESS

We start from the board manufactured in the previous exercise. It must be properly cleaned so the remains of resist have been eliminated. We use a piece of cotton and alcohol to do so. Otherwise, the resist makes soldering more difficult.

There are three major steps to follow:

- Drilling
- Component soldering
- Verification

Drilling

We have to make the drills where the component terminals are to be inserted. These drills are usually from 0,2 to 0,5 mm wider than the terminal.

If the process is being carried out by a CNC machine, a drill file has to be generated by the software package.

Soldering

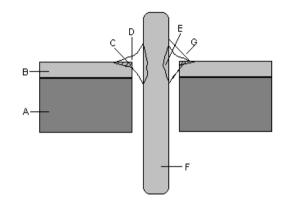
This process intends to create both a mechanical and electrical connection between the components and the board/circuit.

Soldering implies the use of a metal that melts at a relatively low temperature (around 200 °C) to form a molecular bond between the component terminals and the copper tracks. Temperature must be kept low to prevent damaging components and even the adhesive that keeps the copper bound to the base material. A number of alloys are used in electronic soldering. We use the 60-40 tin-lead combination in the lab but the use of lead is banned for industrial purposes where lead free soldering has to be carried out. Melting point is reached at 183 °C in our case.

The oxide present in component terminals and copper tracks is an obstacle for soldering so it must be removed. On this purpose the soldering alloy includes a flux that removes the oxide and protects the soldering.

Around 200 °C, the molten alloy displaces the flux from the surface and creates the molecular bond. This is the moment to stop heating the area and leave it cool naturally.

A good soldering has a bright external aspect and a concave surface. Besides that, the alloy must flow softly covering the surface of both elements that are being soldered. Too much soldering material and big convex droplets indicate that the soldering is no good.



- A. Base material.
- B. Copper layer.
- C. Soldering alloy on touching the copper track
- D. Soldering alloy.
- E. Soldering alloy touching the component terminal.
- F. Terminal.
- G. The angle formed by the alloy and the track must not exceed 30 degrees.

SOLDERING TIPS

Before soldering the IC, insert all terminals.

To prevent components from falling out of their places, bend their terminals 45 degrees before soldering.

After soldering, cut the terminals as short as possible.

Place the tip of the soldering device on the corner formed by the track and the terminal. The soldering thread must be in the same position but not touching the device. This way the alloy will be heated by the terminal ensuring all elements are adequately heated.

Verification

Varnish

A varnish coating can be applied after finishing the process to protect the board from oxidation.

Electrical and mechanical finishing

Once the board has been fully soldered, we just have to install the mechanical elements if any and connect it to external power and signal sources.

Functional test

We need to check that the board is working correctly. If not, try to find and fix the problem.

INSTRUCTIONS FOR THE ELABORATION OF THE EXERCISE REPORT

The report must include:

- Difficulties encountered throughout the process.
- ➤ The final result of the process.
- > Functional test performed and its result.